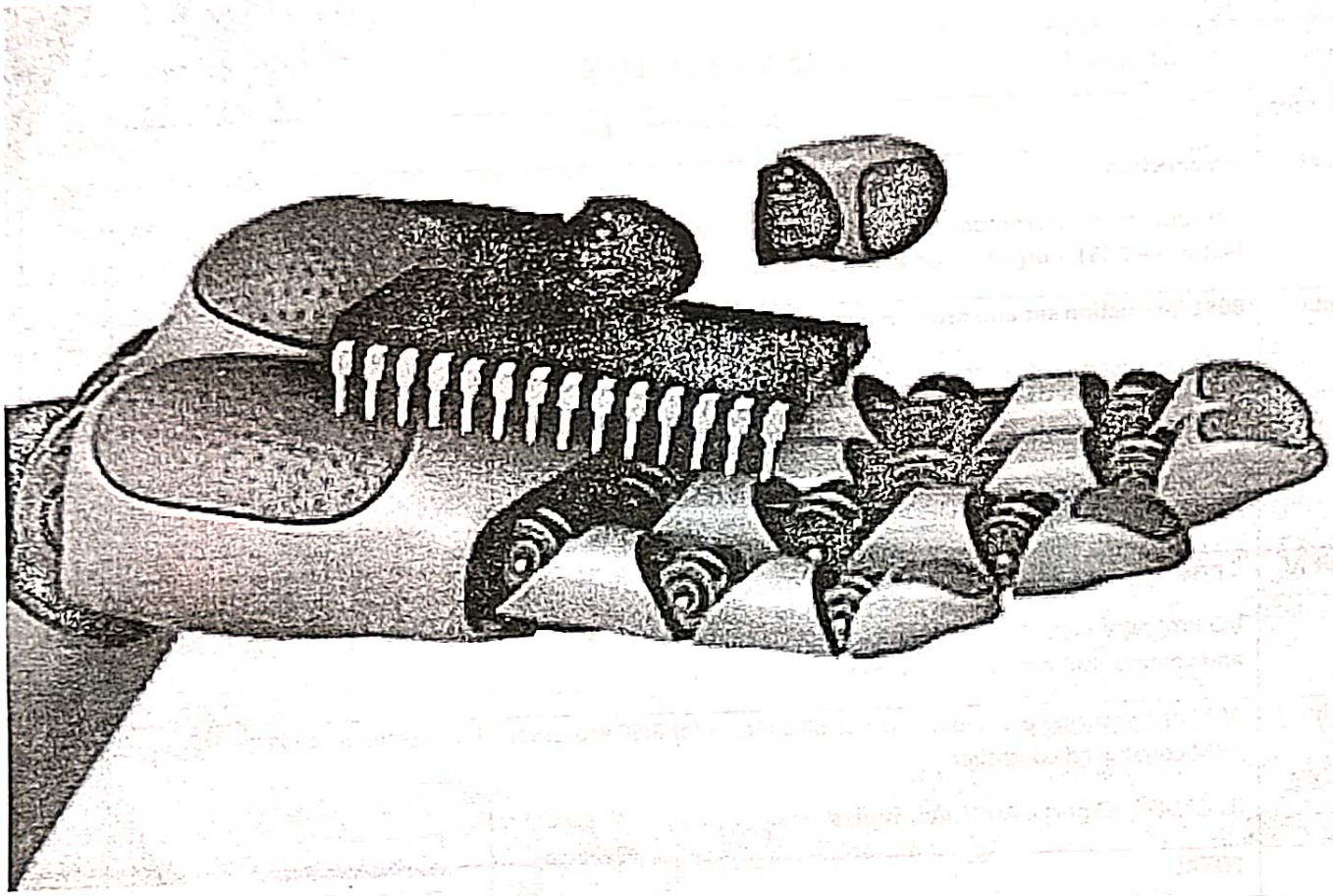


MICROCONTROLLER AND ITS APPLICATIONS

SYLLABUS

Chapter	Name of the Topic	Hours
Unit I	**Introduction** Introduction to Microprocessors and Microcontrollers, Architectures (8085, 8086) Intel MCS51 family features – 8051 – organization and architecture.	10
Unit II	**8051 Instruction set and programming** 8051 instruction set, addressing modes, conditional instructions, I/O Programming, Arithmetic logic instructions, single bit instructions, interrupt handling, programming counters, timers and Stack	12
Unit III	**MCS51 and external Interfaces 8 User interface** – keyboard, LCD, LED, Real world interface – ADC, DAC, SENSORS Communication interface	12
Unit IV	**C programming with 8051** I/O Programming, Timers/counters, Serial Communication, Interrupt, User Interfaces- LCD, Keypad, LED and communication interfaces (RS232).	12
Unit V	ARM processor core based microcontrollers Need for RISC Processor-ARM processor fundamentals, ARM core based controller (LPC214X), IO ports, ADC/DAC, Timers	14
	TOTAL	60

UNIT 01

INTRODUCTION TO MICROPROCESSORS

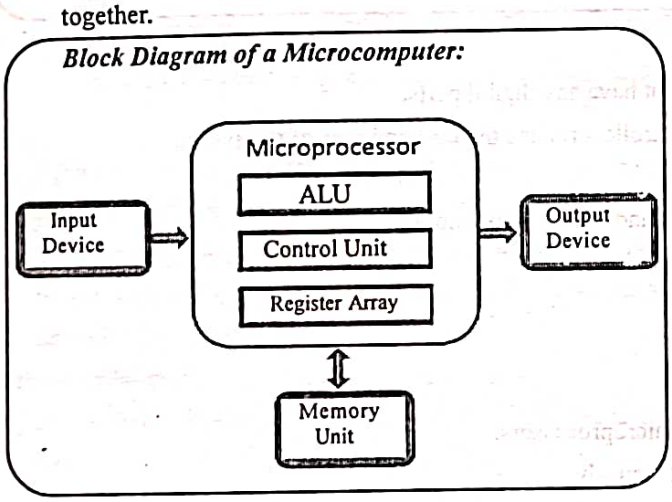
Q.1. Explain Microprocessors. Draw the circuit / block diagram for microprocessors.

Or, Explain Microprocessors and write its advantage, disadvantages and Application.

Ans. Computer's Central Processing Unit (CPU) built on a single Integrated Circuit (IC) is called a microprocessor.

A digital computer with one microprocessor which acts as a CPU is called microcomputer. It is a programmable, multipurpose, clock -driven, register-based electronic device that reads binary instructions from a storage device called memory, accepts binary data as input and processes data according to those instructions and provides results as output. The microprocessor contains millions of tiny components like transistors, registers, and diodes that work together.

Block Diagram of a Microcomputer:



A microprocessor consists of an ALU, control unit and register array. Where ALU performs arithmetic and logical operations on the data received from an input device or memory. Control unit controls the instructions and flow of data within the computer. And, register array consists of registers identified by letters like B, C, D, E, H, L, and accumulator.

Advantages :

The microprocessor is that these are general purpose electronics processing devices which can be programmed to execute a number of tasks

* Compact size
* High speed
* Low power consumption
* It is portable
* It is very reliable
* Less heat generation

Disadvantages :

The main disadvantages are it's overheating physically

* It is only based on machine language
* The overall cost is high
* The large size of PCB is required for assembling all components
* The physical size of the product is big

Overall product design requires more time

A discrete component is used, the system is not reliable

Most of the microprocessor does not support floating point operations

Application of Microprocessor:

Use as Single board Micro Computers

Embedded in PC

Include in Super Minis and CAD

Instrumentation

Controller and many more.

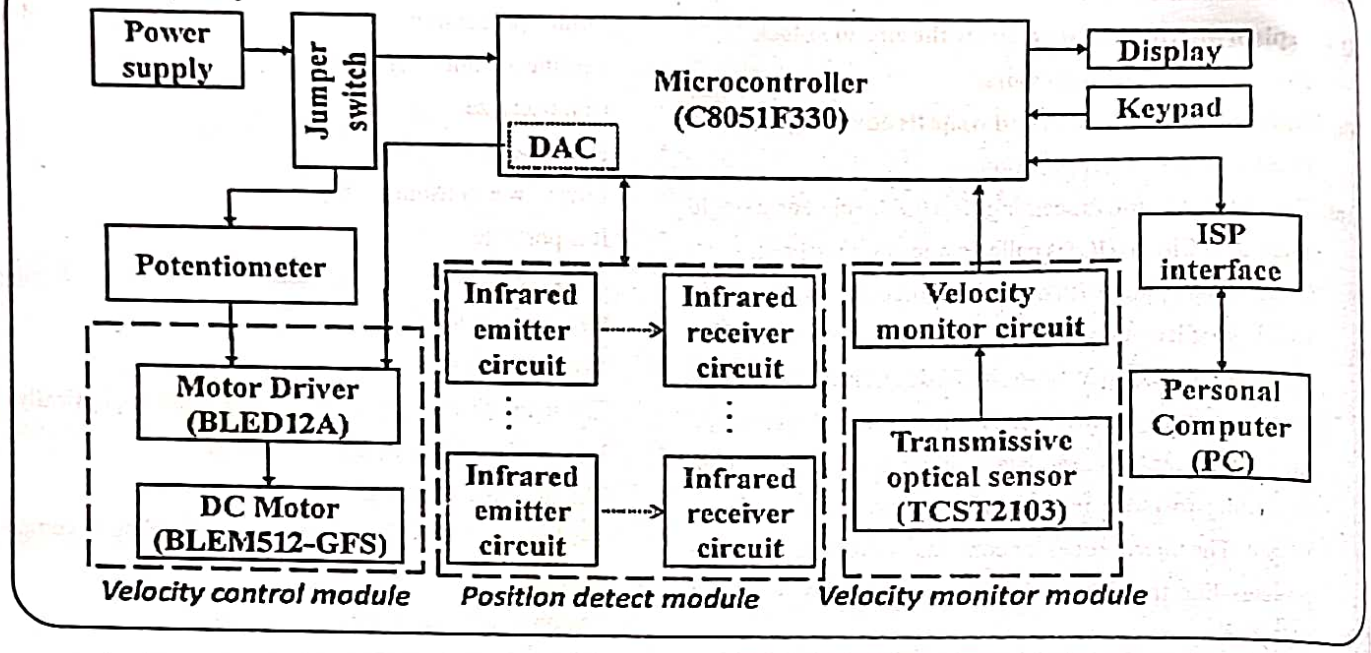
Q.2. Explain Microcontrollers. Draw the circuit / block diagram for microcontrollers.

Or, Explain Microcontrollers and Write its advantage, disadvantages and Application.

Ans. A microcontroller also called MCUs or Microcontroller Unit is a single integrated circuit (IC) that is used for a specific application and designed to implement certain tasks.Products and devices that have been automatically controlled in certain situations, like appliances, power tools, automobile engine control systems, medical equipment,

high-end consumer electronics, rugged industrial devices, and computers are great examples, but microcontrollers reach much higher than these applications.Essentially, a microcontroller works to gather input, process the information, and output a particular action based on the information gathered.Microcontrollers or MCUs can operate at lower speeds, for example, it can operate at around in 1MHz to 200 MHz of range, and is designed to consume less power because they're embedded inside the other devices, which have greater power consumptions in other areas.

Block diagram for Microcontrollers:



Advantages:

Microcontrollers may act as a microcomputer that does not have any digital parts.

Due to the higher integration inside the system, microcontrollers reduce the cost and size of the system.

Instruction cycle timer.

Microcontroller usage is easy, and simple to troubleshoot and system maintaining.

Easily interface additional RAM, ROM, I/O ports.

It required less time for performing operations.

Disadvantages of Microcontrollers

Disadvantages:

Microcontrollers have a more complex architecture than microprocessors.

It can only perform a limited number of executions simultaneously.

- is mostly used in micro-equipments which are hard to operate.

It cannot interface high-power devices directly because of its slower speed.

Applications of Microcontrollers:

Microcontrollers are widely used in various different devices such as -

Light sensing and controlling devices like LED.

Temperature sensing and controlling devices like microwave oven, chimneys.

Fire detection and safety devices like Fire alarm.

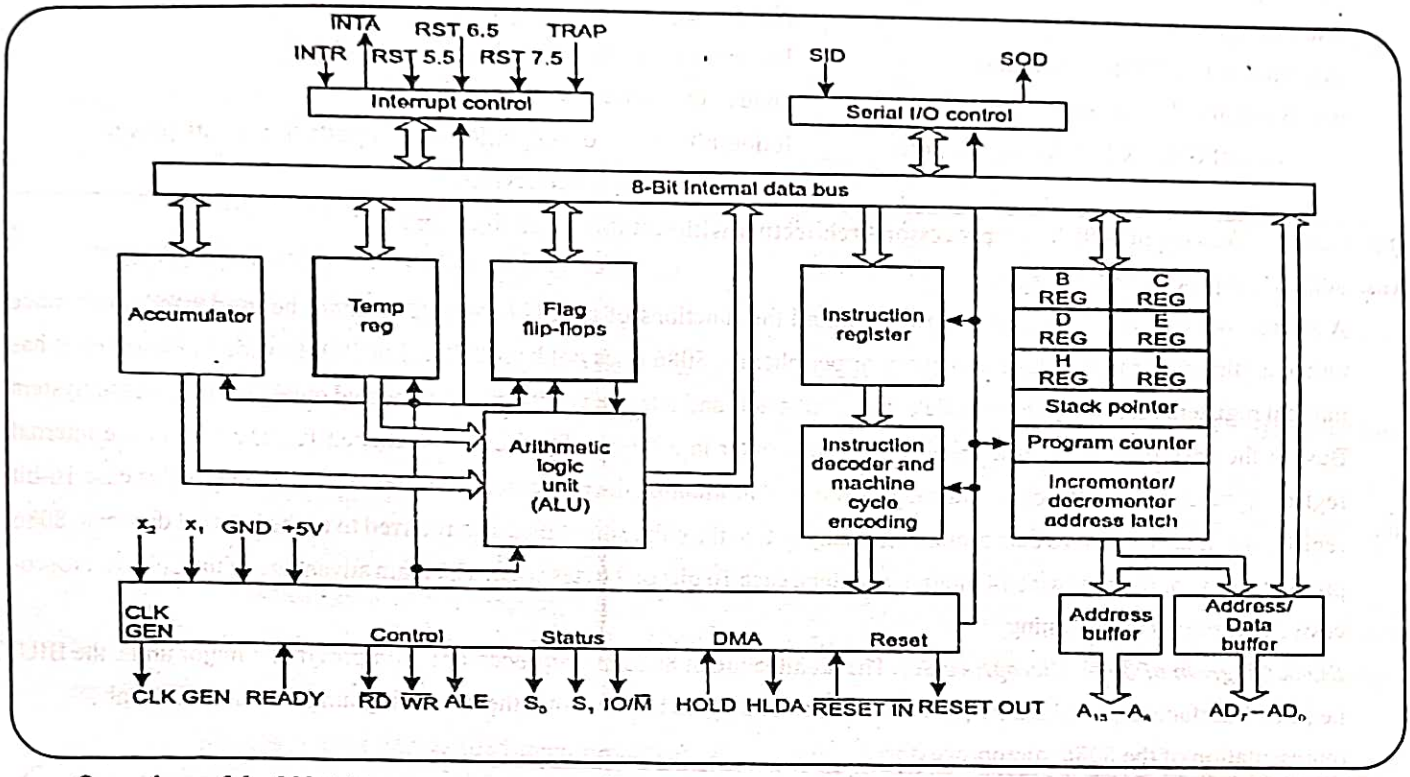
Measuring devices like Volt Meter.

Q.3. Explain Working of 8085 Microprocessor Architecture with suitable block diagram.

Or, Explain 8085 Microprocessor Architecture & Its Applications.

Ans. The 8085 Microprocessor Architecture :

The architecture of the 8085 microprocessor mainly includes the timing & control unit, Arithmetic and logic unit, decoder, instruction register, interrupt control, a register array, serial input/output control. The most important part of the microprocessor is the central processing unit.



Operations of the 8085 Microprocessor: The main operation of ALU is arithmetic as well as logical which includes addition, increment, subtraction, decrement, logical operations like AND, OR, Ex-OR, complement, evaluation, left shift or right shift. Both the temporary registers as well as accumulators are utilized for holding the information throughout the operations then the outcome will be stored within the accumulator. The different flags are arranged or rearrange based on the outcome of the operation.

Applications of the 8085 microprocessor architecture:

As the 8085 microprocessor architecture is included with the instructional set which has multiple basic instructions like Jump, Add, Sub, Move, and others. With this instructional set, instructions are composed in a programming language that is understandable by the operational device and performs numerous functionalities like addition, division, multiplication, moving to carry, and many. Even more complicated can also be done through these microprocessors.

* Engineering Applications.
* Medical Domain.
* Communication.
* Electronics. Etc.

Q4. Write the difference between Microprocessor and Microcontroller.

Ans. The following table highlights the differences between a microprocessor and a microcontroller -

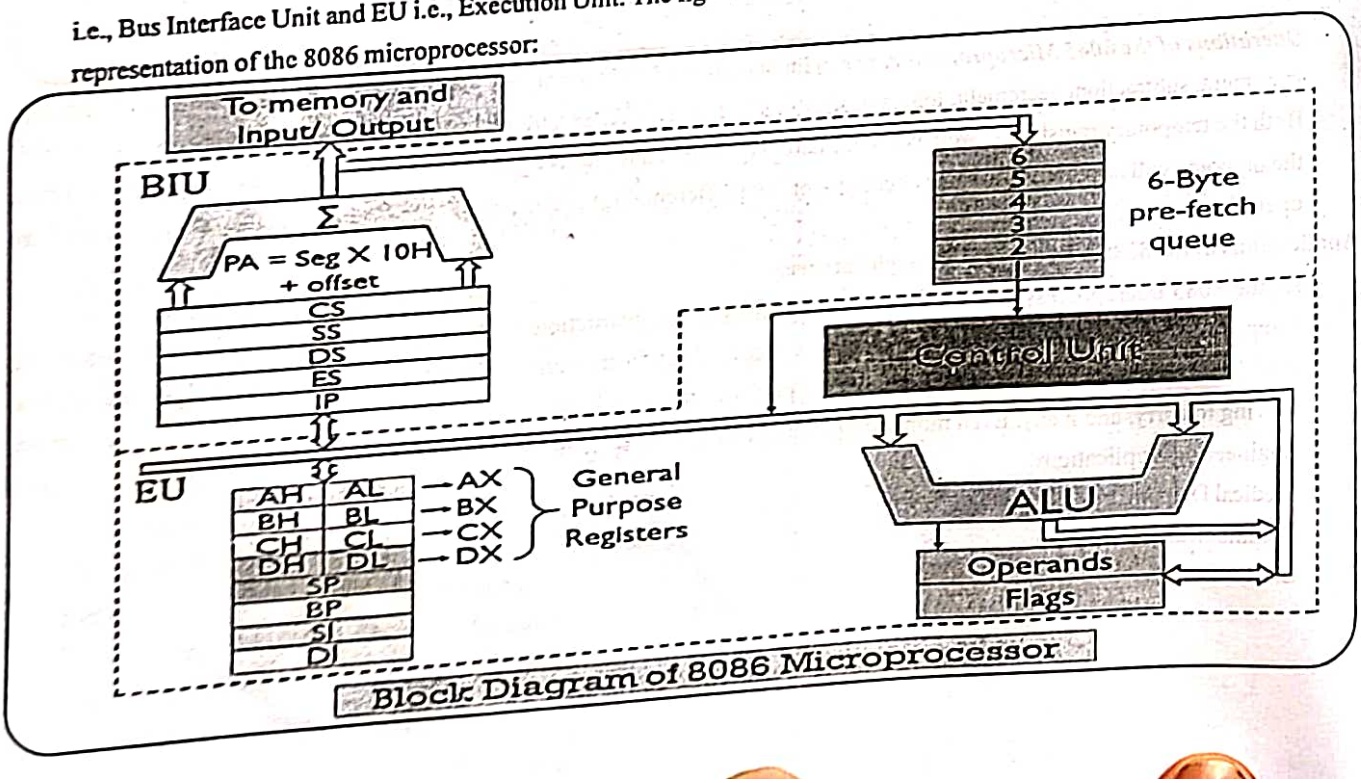
Microprocessor	Microcontroller
Microprocessors are used for big applications.	Microcontrollers are used to execute a single task within an application.
Its designing and hardware cost is high.	Its designing and hardware cost is low.
Not so easy to replace.	Easy to replace.
Its power consumption is high because it has to control the entire system.	It is built with CMOS technology, which requires less power to operate
It doesn't consist of RAM, ROM, I/O ports. It uses its pins to interface to peripheral devices.	It consists of CPU, RAM, ROM, I/O ports.

Q.5. Explain Working of 8086 Microprocessor Architecture with suitable block diagram.

Ans. 8086 Microprocessor Architecture :

A Microprocessor is an Integrated Circuit with all the functions of a CPU however, it cannot be used stand-alone since unlike a microcontroller it has no memory or peripherals. 8086 does not have a RAM or ROM inside it. However, it has internal registers for storing intermediate and final results and interfaces with memory located outside it through the System Bus. In the case of 8086, it is a 16-bit Integer processor in a 40-pin, Dual Inline Packaged IC. The size of the internal registers(present within the chip) indicates how much information the processor can operate on at a time (in this case 16-bit registers) and how it moves data around internally within the chip, sometimes also referred to as the internal data bus. 8086 provides the programmer with 14 internal registers, each 16 bits or 2 bytes wide. The main advantage of the 8086 microprocessor is it supports Pipelining.

Block Diagram of 8086 Microprocessor: The architecture of 8086 microprocessor is composed of 2 major units, the BIU i.e., Bus Interface Unit and EU i.e., Execution Unit. The figure below shows the block diagram of the architectural representation of the 8086 microprocessor:



Block Diagram of 8086 Microprocessor

Bus Interface Unit (BIU): The Bus Interface Unit (BIU) manages the data, address and control buses.The BIU functions in such a way that it:

* Fetches the sequenced instruction from the memory,
* Finds the physical address of that location in the memory where the instruction is stored and
* Manages the 6-byte pre-fetch queue where the pipelined instructions are stored.

An 8086 microprocessor exhibits the property of pipelining the instructions in a queue while performing decoding and execution of the previous instruction. This saves the processor time of operation by a large amount. This pipelining is done in a 6-byte queue. Also, the BIU contains 4 segment registers. Each segment register is 16-bit. The segments are present in the memory and these registers hold the address of all the segments.

Execution Unit (EU): The Execution Unit (EU) performs the decoding and execution of the instructions that are being fetched from the desired memory location.

Control Unit:

Like the timing and control unit in 8085 microprocessor, the control unit in 8086 microprocessor produces control signal after decoding the opcode to inform the general purpose register to release the value stored in it. And it also signals the ALU to perform the desired operation.

ALU:

The arithmetic and logic unit carries out the logical tasks according to the signal generated by the CU. The result of the operation is stored in the desired register.

Flag:

Like in 8085, here also the flag register holds the status of the result generated by the ALU. It has several flags that show the different conditions of the result.

Operand:

It is a temporary register and is used by the processor to hold the temporary values at the time of operation.

The reason behind two separate sections for BIU and EU in the architecture of 8086 is to perform fetching and decoding-executing simultaneously.

Q6. Write the Comparison between 8085 & 8086 Microprocessor.

Ans. Size - 8085 is 8-bit microprocessor, whereas 8086 is 16-bit microprocessor.

Address Bus - 8085 has 16-bit address bus while 8086 has 20-bit address bus.

Memory - 8085 can access up to 64Kb, whereas 8086 can access up to 1 Mb of memory.

Instruction - 8085 doesn't have an instruction queue, whereas 8086 has an instruction queue.

Pipelining - 8085 doesn't support a pipelined architecture while 8086 supports a pipelined architecture.

I/O - 8085 can address 2^8 = 256 I/O's, whereas 8086 can access 2^16 = 65,536 I/O's.

Cost - The cost of 8085 is low whereas that of 8086 is high.

Q.7. Describe the Intel MCS51 family features – 8051 – organization and architecture.

Ans. The 8051 is the original member of the MCS-51 family, and is the core for all MCS-51 devices. The features of the 8051 core are:

* 8-bit CPU optimized for control applications
* Extensive Boolean processing (single-bit logic) capabilities
* 64K Program Memory address space
* 64K Data Memory address space
* On-chip Program Memory
* 128 bytes of on-chip Data RAM
* 32 bidirectional and individually addressable I/O lines
* Two 16-bit timer/counters
* Full duplex UART
* 6-source/5-vector interrupt structure with two priority levels
* On-chip clock oscillator

The basic architectural structure of this 8051 core is shown in Figure 1.

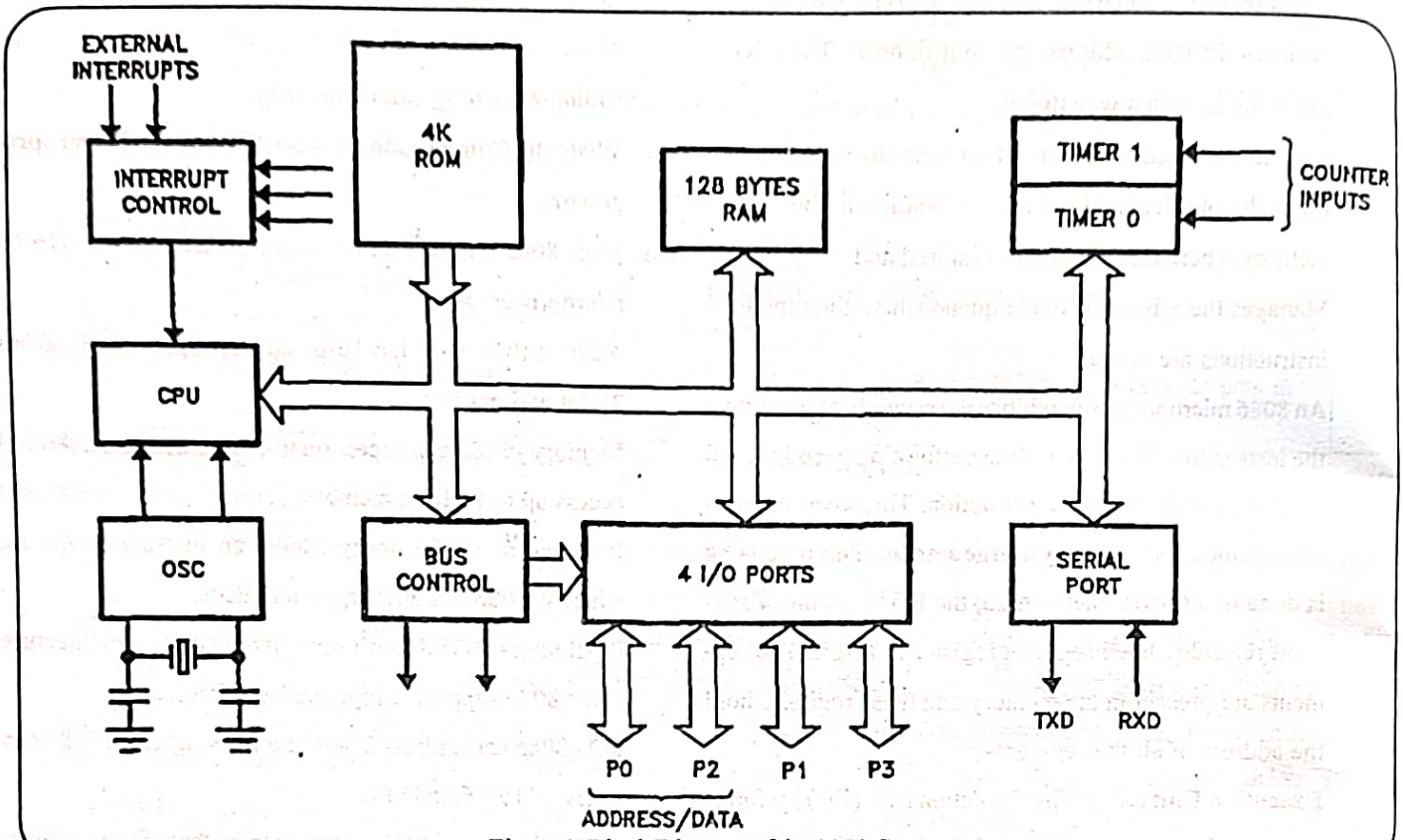


Figure 1. Block Diagram of the 8051 Core.

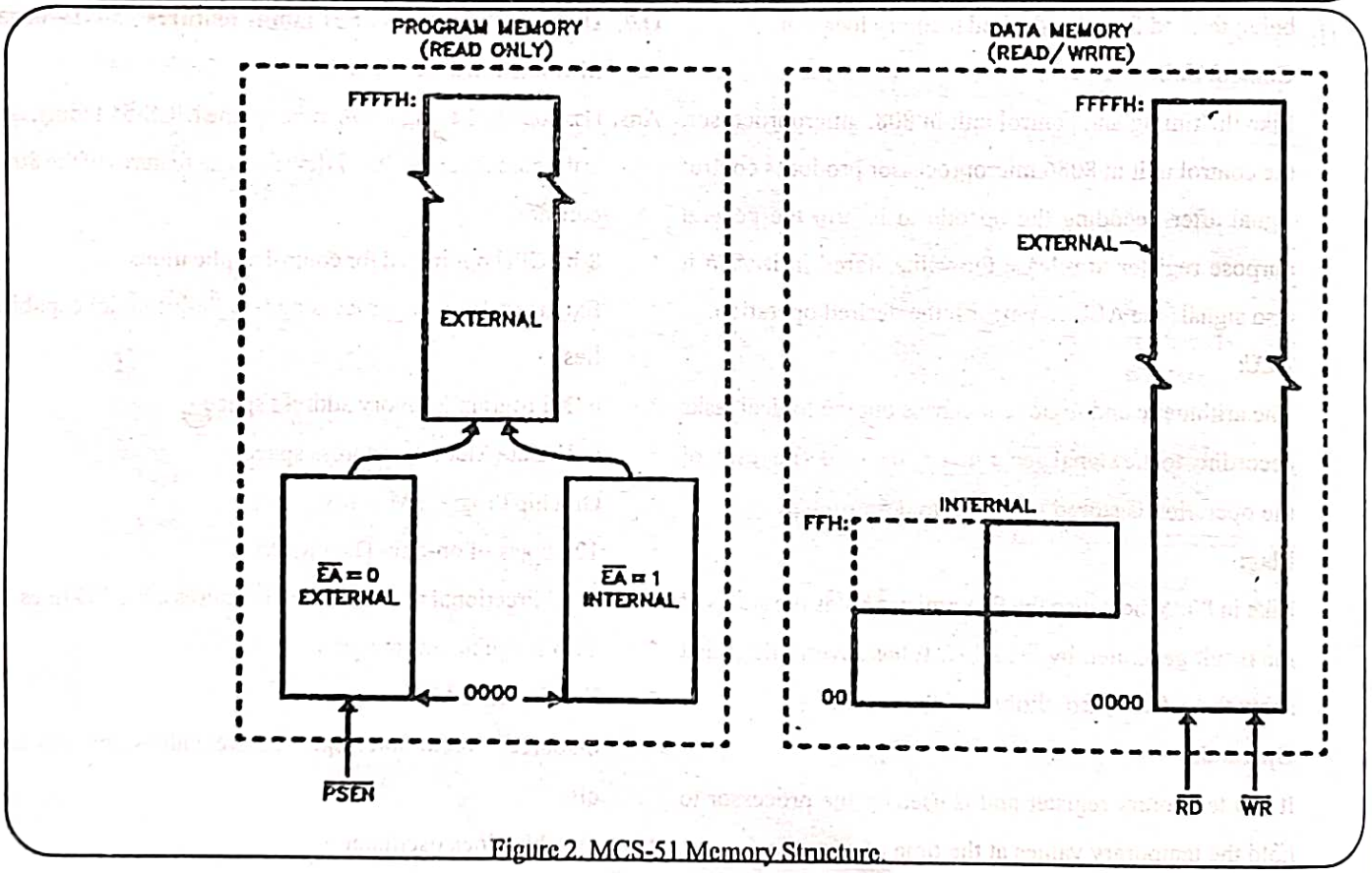


Figure 2. MCS-51 Memory Structure.

8051 – organization:

Logical Separation of Program and Data Memory All MCS-51 devices have separate address spaces for Program and Data Memory, as shown in Fig. 2. The logical separation of Program and Data Memory allows the Data Memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit Data Memory addresses can also be generated through the DPTR register.

Program Memory can only be read, not written to. There can be up to 64K bytes of Program Memory. In the ROM and EPROM versions of these devices the lowest 4K, 8K or 16K bytes of Program Memory are provided on-chip. Refer to Table 1 for the amount of on-chip ROM (or EPROM) on each device. In the ROMless versions all Program Memory is external. The read strobe for external Program Memory is the signal PSEN (Program Store Enable). Data Memory occupies a separate address space from Program Memory. Up to 64K bytes of external RAM can be addressed in the external Data Memory space.

The CPU generates read and write signals, RD and WR, as needed during external Data Memory accesses. External Program Memory and external Data Memory may be combined if desired by applying the RD and PSEN signals to the inputs of an AND gate and using the output of the gate as the read strobe to the external Program/Data memory.

Program Memory:

Figure 3 shows a map of the lower part of the Program Memory. After reset, the CPU begins execution from location 0000H. As shown in Figure 3, each interrupt is assigned a fixed location in Program Memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

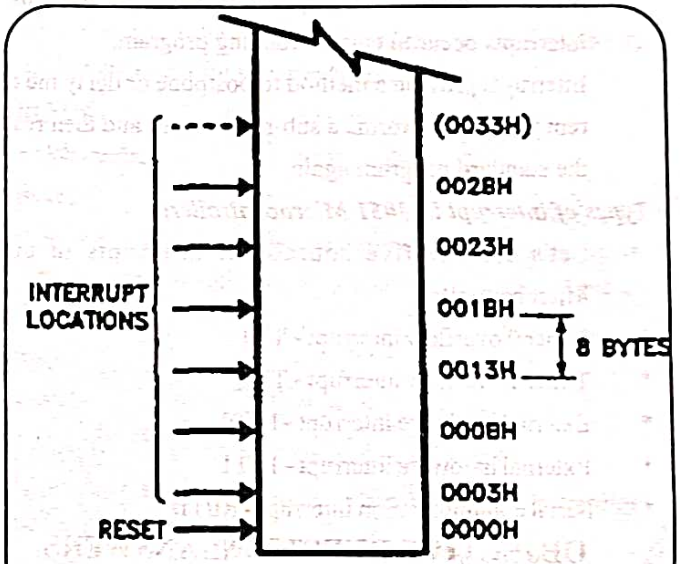
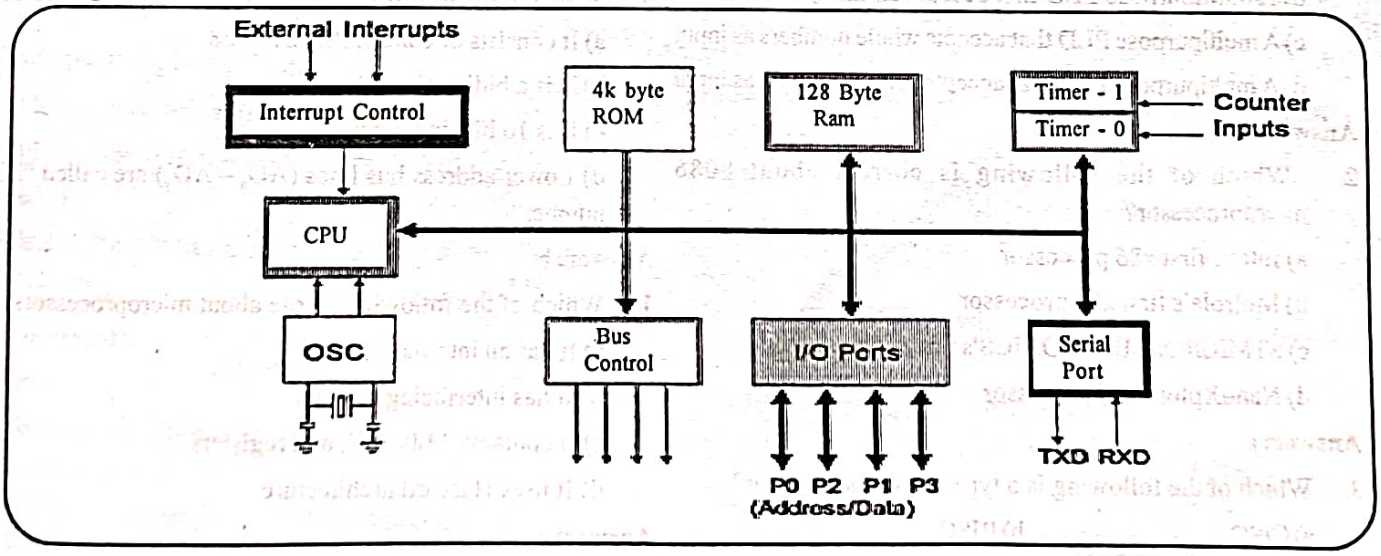


Figure 3. MCS-51 Program Memory

8051 Microcontroller Architecture: Let's see the internal architecture of 8051 Microcontroller represented in form of block diagram as shown below:



Basic components present internally inside 8051 Microcontroller architecture are:

CPU (Central Processing Unit): CPU act as a mind of any processing machine. It synchronizes and manages all processes that are carried out in microcontroller. User has no power to control the functioning of CPU. It interprets the program stored in ROM and carries out from storage and then performs it projected duty. CPU manage the different types of registers available in 8051 microcontroller.

Interrupts: Interrupts is a sub-routine call that given by the microcontroller when some other program with high priority is request for acquiring the system buses the n interrupts occur in current running program.

Interrupts provide a method to postpone or delay the current process, performs a sub-routine task and then restart the standard program again.

Types of interrupt in 8051 Microcontroller:

Let's see the five sources of interrupts in 8051 Microcontroller:

* Timer 0 overflow interrupt - TF0
* Timer 1 overflow interrupt - TF1
* External hardware interrupt - INT0
* External hardware interrupt - INT1
* Serial communication interrupt - RI/TI.

OBJECTIVE QUESTIONS ANSWERS

1. What is Microprocessor?
   a) A multipurpose PLD that accepts binary data as input
   b) A multipurpose PLD that accepts an integer as input
   c) A multipurpose PLD that accepts whole numbers as input
   d) A multipurpose PLD that accepts prime numbers as input

Answer: a

2. Which of the following is correct about 8086 microprocessor?
   a) Intel's first x86 processor
   b) Motrola's first x86 processor
   c) STMICROELECTRONICS's first x86 processor
   d) NanoXplore x86 processor

Answer: a

3. Which of the following is a type of microprocessor?
   a) CISC b) RISC
   c) EPIC d) All of the mentioned

Answer: d

4. The microprocessor of a computer can operate on any information if it is present in _____ only.
   a) Program Counter b) Flag
   c) Main Memory d) Secondary Memory

Answer: c

5. Which of the following technology was used by Intel to design its first 8-bit microprocessor?
   a) NMOS b) HMOS
   c) PMOS d) TTL

Answer: c

6. Which of the following addressing method does the instruction, MOV AX,[BX] represent?
   a) register indirect addressing mode
   b) direct addressing mode
   c) register addressing mode
   d) register relative addressing mode

Answer: a

7. What is the word length of an 8-bit microprocessor?
   a) 8-bits – 64 bits b) 4-bits – 32 bits
   c) 8-bits – 16 bits d) 8-bits – 32 bits

Answer: a

8. In 8-bit microprocessor, how many opcodes are present?
   a) 246 b) 278
   c) 250 d) 256

Answer: a

9. Which of the following is not true about the address bus?
   a) It consists of control PIN 21 to 28
   b) It is a bidirectional bus
   c) It is 16 bits in length
   d) Lower address bus lines ($AD_0 - AD_7$) are called "Line number"

Answer: b

10. Which of the following is true about microprocessors?
    a) It has an internal memory
    b) It has interfacing circuits
    c) It contains ALU, CU, and registers
    d) It uses Harvard architecture

Answer: c

11. Which of the following is the correct sequence of operations in a microprocessor?
    a) Opcode fetch, memory read, memory write, I/O read, I/O write
    b) Opcode fetch, memory write, memory read, I/O read, I/O write
    c) I/O read, opcode fetch, memory read, memory write, I/O write
    d) I/O read, opcode fetch, memory write, memory read, I/O write

Answer: a

12. The _____ directive instructs the assembler to begin memory allocation for a segment/block/code from the stated address.
    a) GROUP b) OFFSET
    c) ORG d) LABEL

Answer: c

13. Which of the following is not a microprocessor?
    a) Z8000 b) Motorola 6809
    c) Zilog Z8 d) PIC1x

Answer: d

14. Which of the following is not a property of TRAP interrupt in microprocessor?
    a) It is a non-maskable interrupt
    b) It is of highest priority
    c) It uses edge-triggered signal
    d) It is a vectored interrupt

Answer: c

15. Which of the following is a property of RST 7.5 interrupt?
    a) It is a non-maskable interrupt
    b) It has 3rd highest priority
    c) It uses level-triggered signal
    d) Its vectored address is 003C H

Answer: d

16. Which of the following flag is used to mask INTR interrupt?
    a) zero flag b) auxiliary carry flag flag
    c) interrupt flag d) sign flag

Answer: c

17. Which of the following is a special-purpose register of microprocessor?
    a) Program counter b) Instruction register
    c) Accumulator d) Temporary register

Answer: a

18. Which of the following circuit is used as a special signal to demultiplex the address bus and data bus?
    a) Priority Encoder b) Decoder
    c) Address Latch Enable d) Demultiplexer

Answer: c

19. How many flip-flops are there in a flag register of 8085 microprocessor?
    a) 4 b) 5
    c) 7 d) 10

Answer: b

20. Which of the following flag condition is used for BCD arithmetic operations in microprocessor?
    a) Sign flag b) Auxiliary carry flag
    c) Parity flag d) Zero flag

Answer: b

21. Whenever a non-maskable interrupt occurs in 8085 microprocessor, which of the following data line contains the data?
    a) 2C H b) 3C H
    c) 36 H d) 24 H

Answer: d

22. What does a microprocessor understand after decoding opcode?
    a) Perform ALU operation
    b) Go to memory
    c) Length of the instruction and number of operations
    d) Go to the output device

Answer: c

23. How many address lines are present in 8086 microprocessor?
    a) 16 b) 20
    c) 32 d) 40

Answer: b

24. Which of the following is not a status flag in microprocessor?
    a) Overflow flag b) Direction flag
    c) Interrupt flag d) Index flag

Answer: d

25. Which of the following is not a condition flag?

a) Trap flag b) Auxiliary carry flag
c) Parity flag d) Zero flag

Answer: a

26. Which of the following register is not used in opcode fetch operations?
a) Program counter b) Memory address register
c) Memory data register d) Flag register

Answer: d

27. A memory connected to a microprocessor has 20 address lines and 16 data lines. What will be the memory capacity?
a) 8 KB b) 2 MB
c) 16 MB d) 64 KB

Answer: b

28. What is the word length of the Pentium-II microprocessor?
a) 8-bit b) 32-bit
c) 64-bit d) 16-bit

Answer: c

29. Which of the following is not true about 8085 microprocessor?
a) It is an 8-bit microprocessor
b) It is a 40 pin DIP chip
c) It is manufactured using PMOS technology
d) It has 16 address lines

Answer: c

30. Which of the following is a non-vectored input?
a) TRAP b) RST-7.5
c) RST-6.5 d) INTR

Answer: d

31. Which of the following is true?
a) Every instruction has two parts i.e. opcode and operands
b) MOV B, C is a two-byte instruction
c) MVI A, 90H is a three-byte instruction
d) Maximum number of T-states possible for the execution of an instruction is 16

Answer: a

32. Which of the following addressing mode is used by 8085 microprocessor for array and list operations?
a) Base-Register b) Direst
c) Indexed d) Immediate

Answer: c

33. What is stored in the H & L general-purpose register?
a) Opcode b) Address of memory
c) Address of next instruction
d) Temporary data

Answer: b

34. If a 90 GB memory has to be connected to a microprocessor, minimum how many address lines are required?
a) 36 b) 39
c) 32 d) 37

Answer: d

35. Which of the following is a software interrupt?
a) TRAP b) INTR
c) RST-6.5 d) RST-5

Answer: d

36. What is the vectored address of RST-5?
a) 0010 H b) 0032 H
c) 0028 H d) 0030 H

Answer: c

37. Which of the following is true about stack pointer?
a) Stack pointer contains the address of the top of the stack memory
b) Stack pointer is an 8-bit register
c) Stack pointer stores data permanently
d) Stack pointer is initialized after stack operation

Answer: a

38. How many address lines are required to connect a 4 KB RAM to a microprocessor?
a) 10 b) 16
c) 12 d) 20

Answer: c

39. Which of the following is true about MOV A, B instruction?
a) It means move the content of register A to register B
b) It uses immediate addressing mode
c) It doesn't affect the flag register
d) It is a 2-byte instruction

Answer: c

40. Which of the following is false about LDA instruction?
a) It is a 3-byte instruction
b) It uses indirect addressing mode
c) It has 13 T-states
d) It doesn't affect any flags

Answer: b

UNIT 02

8051 INSTRUCTION SET AND PROGRAMMING

Q.1. Explain MCS-51 instruction set.

Ans. The MCS-51 Instruction set :

All members of the MCS-51 family execute the same instruction set. The MCS-51 instruction set is optimized for 8-bit control applications. It provides a variety of fast addressing modes for accessing the internal RAM to facilitate byte operations on small data structures. The instruction set provides extensive support for one-bit variables as a separate data type, allowing direct bit manipulation in control and logic systems that require Boolean processing.

An overview of the MCS-51 instruction set is presented below, with a brief description of how certain instructions might be used. References to "the assembler" in this discussion are to Intel's MCS-51 Macro Assembler, ASM51. More detailed information on the instruction set can be found in the MCS-51 Macro Assembler User's Guide (Order No. 9800937 for ISIS Systems, Order No. 122752 for DOS Systems)

Q.2. Explain Addressing Modes.

Ans. The addressing modes in the MCS-51 instruction set are as follows:

1. ***DIRECT ADDRESSING***

In direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal Data RAM and SFRs can be directly addressed.

2. ***INDIRECT ADDRESSING***

In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer.

The address register for 16-bit addresses can only be the 16-bit "data pointer" register, DPTR.

Q3. Explain Conditional instructions or Embedded Systems - Instructions.

Ans. The flow of program proceeds in a sequential manner, from one instruction to the next instruction, unless a control transfer instruction is executed. The various types of control transfer instruction in assembly language include conditional or unconditional jumps and call instructions.

Loop and Jump Instructions

Looping in the 8051: Repeating a sequence of instructions a certain number of times is called a loop. An instruction DJNZ reg, label is used to perform a Loop operation. In this instruction, a register is decremented by 1; if it is not zero, then 8051 jumps to the target address referred to by the label.The register is loaded with the counter for the number of repetitions prior to the start of the loop. In this instruction, both the registers decrement and the decision to jump are combined into a single instruction. The registers can be any of R0–R7. The counter can also be a RAM location.

Other Conditional Jumps :The following table lists the conditional jumps used in 8051 -

Instruction	Action
JZ	Jump if A = 0
JNZ	Jump if A $\neq$ 0
DJNZ	Decrement and Jump if register $\neq$ 0
CJNE A, data	Jump if A $\neq$ data
CJNE reg, #data	Jump if byte $\neq$ data
JC	Jump if CY = 1
JNC	Jump if CY $\neq$ 1
JB	Jump if bit = 1
JNB	Jump if bit = 0
JBC	Jump if bit = 1 and clear bit

* JZ (jump if A = 0) - In this instruction, the content of the accumulator is checked. If it is zero, then the 8051 jumps

UNIT 02

8051 INSTRUCTION SET AND PROGRAMMING

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In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer.

The address register for 16-bit addresses can only be the 16-bit "data pointer" register, DPTR.

Q3. Explain Conditional instructions or Embedded Systems - Instructions.

Ans. The flow of program proceeds in a sequential manner, from one instruction to the next instruction, unless a control transfer instruction is executed. The various types of control transfer instruction in assembly language include conditional or unconditional jumps and call instructions.

Loop and Jump Instructions

Looping in the 8051: Repeating a sequence of instructions a certain number of times is called a loop. An instruction DJNZ reg, label is used to perform a Loop operation. In this instruction, a register is decremented by 1; if it is not zero, then 8051 jumps to the target address referred to by the label.The register is loaded with the counter for the number of repetitions prior to the start of the loop. In this instruction, both the registers decrement and the decision to jump are combined into a single instruction. The registers can be any of R0–R7. The counter can also be a RAM location.

Other Conditional Jumps :The following table lists the conditional jumps used in 8051 -

Instruction	Action
JZ	Jump if A = 0
JNZ	Jump if A $\neq$ 0
DJNZ	Decrement and Jump if register $\neq$ 0
CJNE A, data	Jump if A $\neq$ data
CJNE reg, #data	Jump if byte $\neq$ data
JC	Jump if CY = 1
JNC	Jump if CY $\neq$ 1
JB	Jump if bit = 1
JNB	Jump if bit = 0
JBC	Jump if bit = 1 and clear bit

* JZ (jump if A = 0) - In this instruction, the content of the accumulator is checked. If it is zero, then the 8051 jumps

to the target address. JZ instruction can be used only for the accumulator, it does not apply to any other register.

- JNZ (jump if A is not equal to 0) - In this instruction, the content of the accumulator is checked to be non-zero. If it is not zero, then the 8051 jumps to the target address.
- JNC (Jump if no carry, jumps if CY = 0) - The Carry flag bit in the flag (or PSW) register is used to make the decision whether to jump or not "JNC label". The CPU looks at the carry flag to see if it is raised (CY = 1). If it is not raised, then the CPU starts to fetch and execute instructions from the address of the label. If CY = 1, it will not jump but will execute the next instruction below JNC.
- JC (Jump if carry, jumps if CY = 1) - If CY = 1, it jumps to the target address.
- JB (jump if bit is high)
- JNB (jump if bit is low)

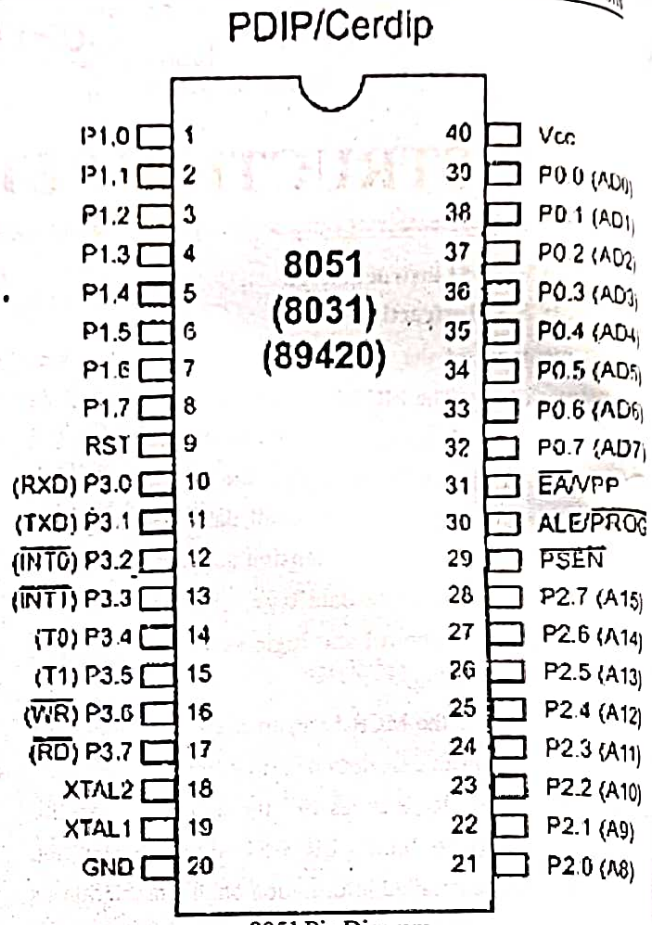
Unconditional Jump Instructions

There are two unconditional jumps in 8051 -

LJMP (long jump) - LJMP is 3-byte instruction in which the first byte represents opcode, and the second and third bytes represent the 16-bit address of the target location. The 2-byte target address is to allow a jump to any memory location from 0000 to FFFFH. SJMP (short jump) - It is a 2-byte instruction where the first byte is the opcode and the second byte is the relative address of the target location. The relative address ranges from 00H to FFH which is divided into forward and backward jumps; that is, within –128 to +127 bytes of memory relative to the address of the current PC (program counter). In case of forward jump, the target address can be within a space of 127 bytes from the current PC. In case of backward jump, the target address can be within –128 bytes from the current PC.

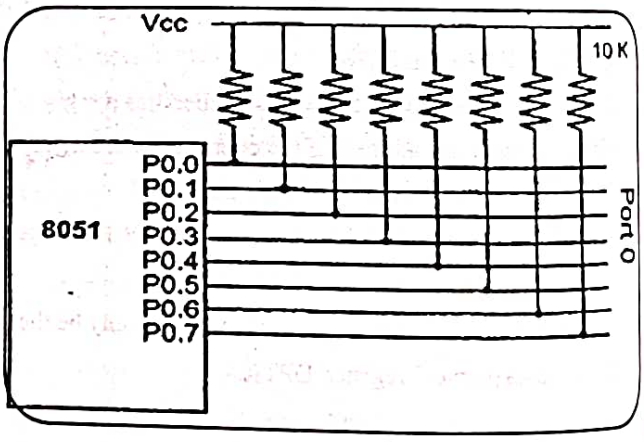
Q4. Explain I/O Programming for 8051.

Ans. *I/O Programming for 8051:* In the 8051 there are a total of four ports for I/O operations. Examining Figure 4-1, note that of the 40 pins, a total of 32 pins are set aside for the four ports PO, PL P2, and P3, where each port takes 8 pins. The rest of the pins are designated as Vrt, GND, XTAL1, XTAL2. RST, EA, ALE/PROG and PSEN are discussed.



8051 Pin Diagram

I/O port pins and their functions: The four ports PO, Pi, P2, and P3 each use 8 pins, making them 8-bit ports. All the ports upon RESET are configured as inputs, ready to be used as input ports. When the first 0 is written to a port, it becomes an output. To reconfigure it as an input, a 1 must be sent to the port. To use any of these ports as an input port, it must be programmed, as we will explain throughout this section. First, we describe each port.



Port 0 occupies a total of 8 pins (pins 32 -39). It can be used for input or output. To use the pins of port 0 as both input and output ports, each pin must be connected externally to a 10K-ohm pull-up resistor. This is due to the fact that P0 is an open drain, unlike P1, P2, and P3, as Figure 4-2. Port 0 with Pull-Up Resistors we will soon see. Open drain is a term used for MOS chips in the same way that open collector is used for TTL chips. In any system using the 8051/52 chip, we normally connect P0 to pull-up resistors. See Figure 4-2. In this way we take advantage of port 0 for both input and output. For example, the following code will continuously send out to port 0 the alternating values of 55H and AAH.

```
;Toggle all bits of P0
BACK:   MOV   A,#55H
        MOV   P0,A
        ACALL DELAY
        MOV   A,#0AAH
        MOV   P0,A
        ACALL DELAY
        SJMP  BACK
```

Q5. Explain Arithmetic instructions ?

Ans. The menu of arithmetic instructions is listed in Table . The table indicates the addressing modes that can be used with each instruction to access the < byte > operand. For example, the ADD A, < byte > instruction can be written as:

ADD A,7FH (direct addressing)
ADD A,@R0 (indirect addressing)
ADD A,R7 (register addressing)
ADD A, ≠ 127 (immediate constant)

The execution times listed in Table assume a 12 MHz clock frequency. All of the arithmetic instructions execute in 1 ms except the INC DPTR instruction, which takes 2 ms, and the Multiply and Divide instructions, which take 4 ms. Note that any byte in the internal Data Memory space can be incremented or decremented without going through the Accumulator. One of the INC instructions operates on the 16-bit Data Pointer. The Data Pointer is used to generate 16-bit addresses for external memory, so being able to increment it in one 16-bit operation is a useful feature. The MUL AB instruction multiplies the Accumulator by the data in the B register and puts the 16-bit product into the concatenated B and Accumulator registers.

Table 2. A List of the MCS®-51 Arithmetic Instructions

Mnemonic	Operation	Addressing Modes				Execution Time (μs)
		Dir	Ind	Reg	Imm	
ADD A,<byte>	A = A + <byte>	X	X	X	X	1
ADDC A,<byte>	A = A + <byte> + C	X	X	X	X	1
SUBB A,<byte>	A = A − <byte> − C	X	X	X	X	1
INC A	A = A + 1	Accumulator only				1
INC <byte>	<byte> = <byte> + 1	X	X	X		1
INC DPTR	DPTR = DPTR + 1	Data Pointer only				2
DEC A	A = A − 1	Accumulator only				1
DEC <byte>	<byte> = <byte> − 1	X	X	X		1
MUL AB	B:A = B x A	ACC and B only				4
DIV AB	A = Int [A/B] B = Mod [A/B]	ACC and B only				4
DA A	Decimal Adjust	Accumulator only				1

The DIV AB instruction divides the Accumulator by the data in the B register and leaves the 8-bit quotient in the Accumulator, and the 8-bit remainder in the B register. Oddly enough, DIV AB finds less use in arithmetic "divide" routines than in radix conversions and programmable shift operations. An example of the use of DIV AB in a radix conversion will be given later. In shift operations, dividing a number by 2n shifts its n bits to the right. Using DIV AB to perform the division completes the

shift in 4 ms and leaves the B register holding the bits that were shifted out. The DAA instruction is for BCD arithmetic operations. In BCD arithmetic, ADD and ADDC instructions should always be followed by a DA A operation, to ensure that the result is also in BCD. Note that DA

A will not convert a binary number to BCD. The DA A operation produces a meaningful result only as the second step in the addition of two BCD bytes.

Q.6. Describe logic instruction with table ?

Or: Explain arithmatic and logic instruction ?

Or Write short notes of the following :

(1) Arithmatic instruction

(2) Logic instruction

Ans. Airthmatic instruction : See the above answer

Logic instruction : Table 3 shows the list of MCS-51 logical instructions. The instructions that perform Boolean operations (AND, OR, Exclusive OR, NOT) on bytes perform the operation on a bit-by-bit basis. That is, if the Accumulator contains 00110101B and < byte > contains 01010011B, then

ANL A,< byte >

will leave the Accumulator holding 00010001B.

The addressing modes that can be used to access the < byte > operand are listed in Table 3. Thus, the

ANL	A, < byte >	instruction may take any of the forms
ANL	A,7FH	(direct addressing)
ANL	A,@R1	(indirect addressing)
ANL	A,R6	(register addressing)
ANL	A, ≠ 53H	(immediate constant)

All of the logical instructions that are accumulator specific execute in 1ms (using a 12 MHz clock). The others take 2 ms.

If the operation is in response to an interrupt, not using the Accumulator saves the time and effort to stack it in the service routine. The Rotate instructions (RL A, RLC A, etc.) shift the Accumulator 1 bit to the left or right. For a left rotation, the MSB rolls into the LSB position. For a right rotation, the LSB rolls into the MSB position.

The SWAP A instruction interchanges the high and low nibbles within the Accumulator. This is a useful operation in BCD manipulations. For example, if the Accumulator contains a binary number which is known to be less than 100, it can be quickly converted to BCD by the following code:

```
MOV     B, ≠ 10
DIV     AB
SWAP    A
ADD     A,B
```

Dividing the number by 10 leaves the tens digit in the low nibble of the Accumulator, and the ones digit in the B register. The SWAP and ADD instructions move the tens digit to the high nibble of the Accumulator, and the ones digit to the low nibble.

Q7. Explain single bit instructions or Boolean Instruction.

Ans. MCS-51 devices contain a complete Boolean (single-bit) processor. The internal RAM contains 128 addressable bits, and the SFR space can support up to 128 other addressable bits. All of the port lines are bit-addressable and each one can be treated as a separate singlebit port. The instructions that access these bits are not just conditional branches, but a complete menu of move, set, clear, complement, OR, and AND instructions. These kinds of bit operations are not easily obtained in other architectures with any amount of byteoriented software.

Table 7. A List of the MCSÉ-51 Boolean Instructions

Mnemonic		Operation	Execution Time (μs)
ANL	C,bit	C = C .AND. bit	2
ANL	C,/bit	C = C .AND. .NOT. bit	2
ORL	C,bit	C = C .OR. bit	2
ORL	C,/bit	C = C .OR. .NOT. bit	2
MOV	C,bit	C = bit	1
MOV	bit,C	bit = C	2
CLR	C	C = 0	1
CLR	bit	bit = 0	1
SETB	C	C = 1	1
SETB	bit	bit = 1	1
CPL	C	C = .NOT. C	1
CPL	bit	bit = .NOT. bit	1
JC	rel	Jump if C = 1	2
JNC	rel	Jump if C = 0	2
JB	bit,rel	Jump if bit = 1	2
JNB	bit,rel	Jump if bit = 0	2
JBC	bit,rel	Jump if bit = 1; CLR bit	2

The instruction set for the Boolean processor is shown in Table 7.

All bit accesses are by direct addressing. Bit addresses 00H through 7FH are in the Lower 128, and bit addresses 80H through FFH are in SFR space. Note how easily an internal flag can be moved to a port pin:

```
MOV     C, FLAG
MOV     P1.0,C
```

In this example, FLAG is the name of any addressable bit in the Lower 128 or SFR space. An I/O line (the LSB of Port 1, in this case) is set or cleared depending on whether the flag bit is 1 or 0. The Carry bit in the PSW is used as the single-bit Accumulator of the Boolean processor. Bit instructions that refer to the Carry bit as C assemble as Carry-specific instructions (CLR C, etc). The Carry bit also has a direct address, since it resides in the PSW register, which is bit-addressable. Note that the Boolean instruction set includes ANL and ORL operations, but not the XRL (Exclusive OR) operation. An XRL operation is simple to implement in software. Suppose, for example, it is required to form the Exclusive OR of two bits:

C = bit1 .XRL. bit2

The software to do that could be as follows:

```
MOV     C,bit1
JNB bit2,OVER
CPL C
OVER: (continue)
```

First, bit1 is moved to the Carry. If bit2 = 0, then C now contains the correct result. That is, bit1 .XRL. bit2 = bit1 if bit2 = 0. On the other hand, if bit2 = 1 C now contains the complement of the correct result. It need only be inverted (CPL C) to complete the operation. This code uses the JNB instruction, one of a series of bit-test instructions which execute a jump if the addressed bit is set (JC, JB, JBC) or if the addressed bit is not set (JNC, JNB). In the above case, bit2 is being tested, and if bit2 = 0 the CPL C instruction is jumped over. JBC executes the jump if the addressed bit is set, and also clears the bit. Thus a flag can be tested and cleared in one operation. All the PSW bits are directly addressable, so the Parity bit, or the general purpose flags, for example, are also available to the bit-test instructions.

Q8. Describe interrupt handling or interrupt Control System.

Ans. Interrupt handling system. : The 8051 core provides 5 interrupt sources: 2 external interrupts, 2 timer interrupts, and the serial port interrupt. What follows is an overview of the interrupt structure for the 8051. Other MCS-51 devices have additional interrupt sources and vectors as shown in Table 1. Refer to the appropriate chapters on other devices for further information on their interrupts.

INTERRUPT ENABLES : Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the SFR

(MSB)							(LSB)
EA	—	—	ES	ET1	EX1	ET0	EX0

Enable bit = 1 enables the interrupt.
Enable bit = 0 disables it.

Symbol	Position	Function
EA	IE.7	disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	reserved*
—	IE.5	reserved*
ES	IE.4	Serial Port Interrupt enable bit.
ET1	IE.3	Timer 1 Overflow Interrupt enable bit.
EX1	IE.2	External Interrupt 1 enable bit.
ET0	IE.1	Timer 0 Overflow Interrupt enable bit.
EX0	IE.0	External Interrupt 0 enable bit.

*These reserved bits are used in other MCS-51 devices.

Fig.(a) IE (Interrupt Enable)Register in the 8051

Named IE (Interrupt Enable). This register also contains a global disable bit, which can be cleared to disable all interrupts at once. Fig.(a) shows the IE register for the 8051.

INTERRUPT PRIORITIES : Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in the SFR named IP (Interrupt Priority). Fig.(b) shows the IP register in the 8051. A low-priority interrupt can be interrupted by a highpriority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted byany other interrupt source. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence. Fig.(c) shows, for the 8051, how the IE and IP registers and the polling sequence work to determine which if any interrupt will be serviced.

(MSB)							(LSB)
—	—	—	PS	PT1	PX1	PT0	PX0

Priority bit = 1 assigns high priority.
Priority bit = 0 assigns low priority.

Symbol	Position	Function
—	IP.7	reserved*
—	IP.6	reserved*
—	IP.5	reserved*
PS	IP.4	Serial Port interrupt priority bit.
PT1	IP.3	Timer 1 interrupt priority bit.
PX1	IP.2	External Interrupt 1 priority bit.
PT0	IP.1	Timer 0 interrupt priority bit.
PX0	IP.0	External Interrupt 0 priority bit.

*These reserved bits are used in other MCS-51 devices.

Fig.(b). IP (Interrupt Priority)Register in the 8051

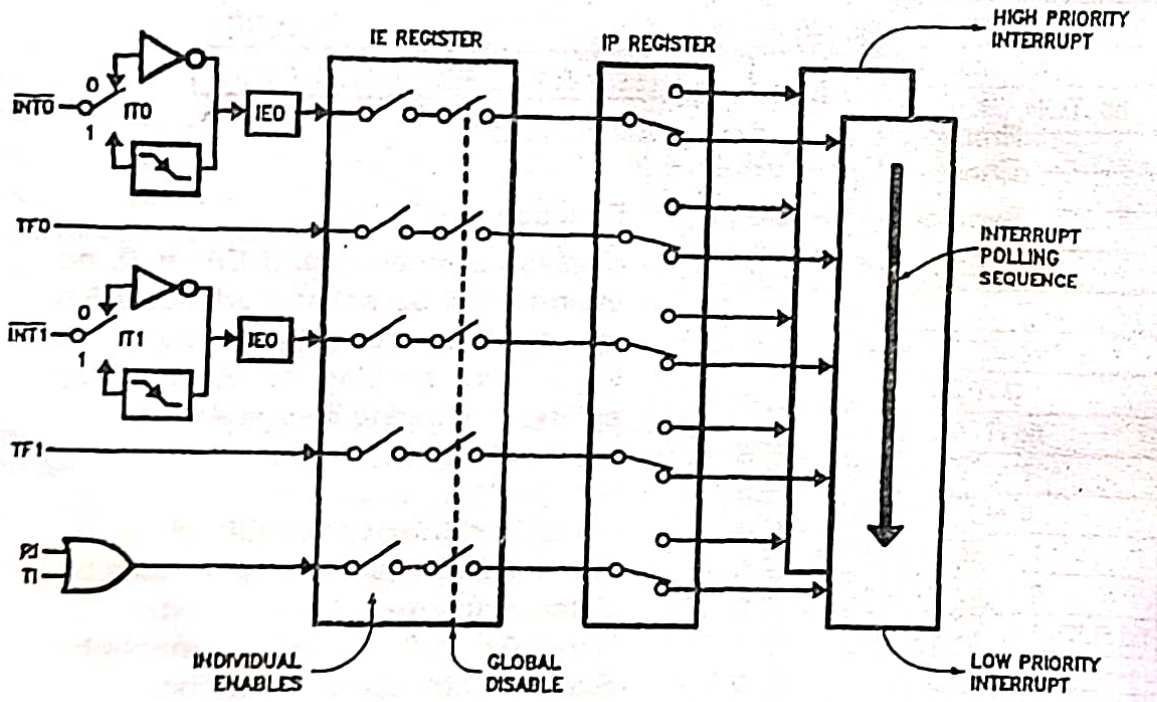


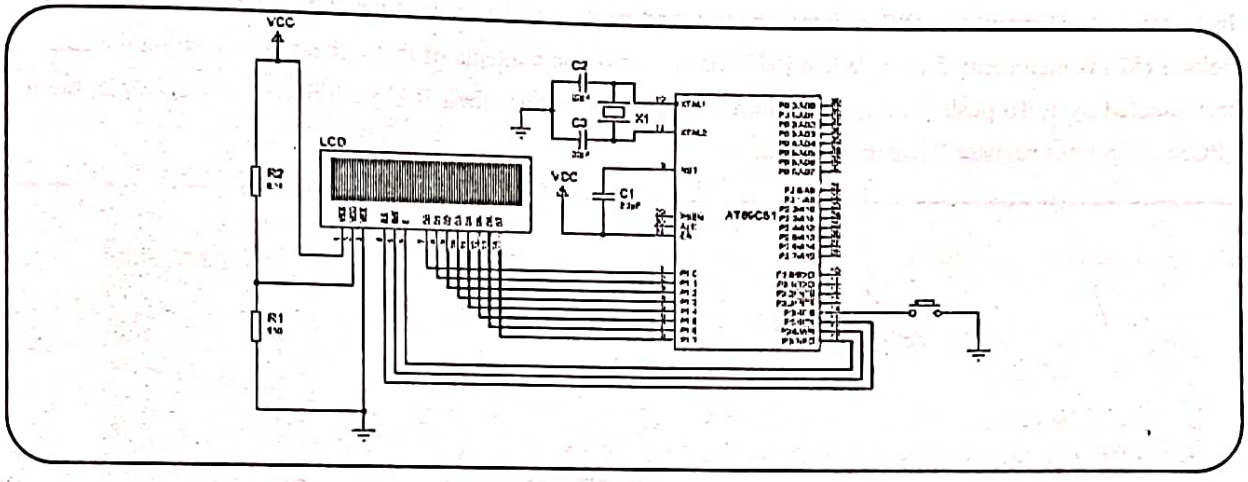
Fig.(c). 8051 Interrupt Control System

In operation, all the interrupt flags are latched into the interrupt control system during State 5 of every machine cycle. The

samples are polled during the following machine cycle. If the flag for an enabled interrupt is found to be set (1), the interrupt system generates an LCALL to the appropriate location in Program Memory, unless some other condition blocks the interrupt. Several conditions can block an interrupt, among them that an interrupt of equal or higher priority level is already in progress. The hardware-generated LCALL causes the contents of the Program Counter to be pushed onto the stack, and reloads the PC with the beginning address of the service routine. As previously noted (Figure 3), the service routine for each interrupt begins at a fixed location. Only the Program Counter is automatically pushed onto the stack, not the PSW or any other register. Having only the PC be automatically saved allows the programmer to decide how much time to spend saving which other registers. This enhances the interrupt response time, albeit at the expense of increasing the programmer's burden of responsibility. As a result, many interrupt functions that are typical in control applicationsÐtoggling a port pin, for example, or reloading a timer, or unloading a serial bufferÐcan often be completed in less time than it takes other architectures to commence them.

Q9. Explain Programming Counters in 8051 Microcontroller.

Ans. Programming Counters in 8051 is used to count the external events through the T0 & T1 pins in the controller. Counters counts the external clock source whereas the timers counts the clock source from the oscillator used. The concept of counters play an important role where the embedded designer needs to count the number of events taking place by feeding clock per events.



Q10. Describe Frequency counting program - Timers in 8051.

Ans. This program written above is to count the frequency of pulse which is present at the pin p3.4. we are using timer 0 as counter, and timer 1 as normal timer.in line 10, the control wastes around 35.75 ms, so in order to make timer 0 active for around 1 second, we are using line 10 for 28 times.

```
        ORG   0000H
RPT:    MOV   TMOD,#15H      ;timer 1 as timer and Timer 0 as counter
        SETB  P3.4           ;make port P3.4 an input port
        MOV   TL0,#00        ;clear TL0
        MOV   TH0,#00        ;clear TH0
        SETB  TR0            ;start counter
        MOV   R0,#28         ;R0=28,to time 1 second
AGAIN:  MOV   TL1,#00H       ;TL1=0
        MOV   TH1,#00H       ;TH1=0
        SETB  TR1            ;start Timer 1
BACK:   JNB   TF1,BACK       ;test Timer 1 flag
        CLR   TF1            ;clear Timer 1 flag
        CLR   TR1            ;stop Timer 1
        DJNZ  R0,AGAIN       ;repeat the loop until R0=0
        MOV   A,TL0          ;since 1 sec has elapsed, check TL0
        MOV   P2,A           ;move TL0 to port 2
        MOV   A,TH0          ;move TH0 to ACC
        MOV   P1,A           ;move it to port 1
        SJMP  RPT            ;repeat
        END
```

But here in the image in line 14 they referenced the DJNZ to line 8, why? What is the the point of refilling the register with 00 again? They could have simply clear the TF1 to start the timer again from 00 instead they are stopping the timer in line 13, and again restarting it after filling with 00. What is the need of stopping the timer and refill it again with 00? Won't just clearing the TF1 (While keeping TR1 is set) make the timer again start counting from 00? Since the roll over value is already 00 and loaded in the timer after overflow.

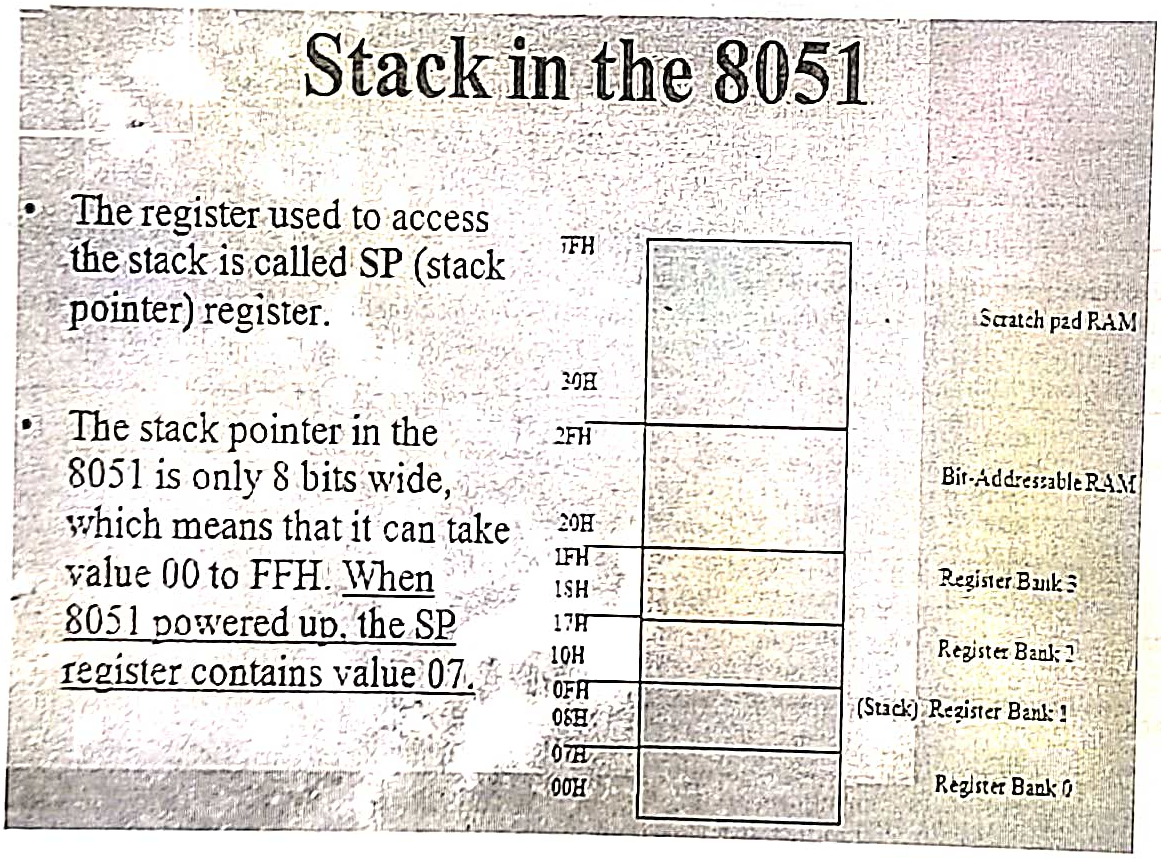
Q11. Explain Stack in the 8051.

Ans. The stack is a section of a RAM used by the CPU to store information such as data or memory address on temporary basis. The CPU needs this storage area considering limited number of registers. How Stacks are Accessed

As the stack is a section of a RAM, there are registers inside the CPU to point to it.

The register used to access the stack is known as the stack pointer register. The stack pointer in the 8051 is 8-bits wide, and it can take a value of 00 to FFH. When the 8051 is initialized, the SP register contains the value 07H. This means that the RAM location 08 is the first location used for the stack. The storing operation of a CPU register in the stack is known as a PUSH, and getting the contents from the stack back into a CPU register is called a POP. Pushing into the Stack

In the 8051, the stack pointer (SP) points to the last used location of the stack. When data is pushed onto the stack, the stack pointer (SP) is incremented by 1. When PUSH is executed, the contents of the register are saved on the stack and SP is incremented by 1. To push the registers onto the stack, we must use their RAM addresses. For example, the instruction "PUSH 1" pushes register R1 onto the stack.



OBJECTIVE QUESTIONS ANSWERS

1. Which of the following is not an instruction of 8051 instructions?
   a) arithmetic instructions b) boolean instructions
   c) logical instructions d) none

Answer: d

2. The operations performed by data transfer instructions are on
   a) bit data b) byte data
   c) 16-bit data d) all of the mentioned

Answer: d

3. Which of the following is true while executing data transfer instructions?
   a) program counter is not accessible
   b) restricted bit-transfer operations are allowed
   c) both operands can be direct/indirect register operands
   d) all of the mentioned

Answer: c

4. The logical instruction that affects the carry flag during its execution is
   a) XRL A;
   b) ANL A;
   c) ORL A;
   d) RLC A;

Answer: d

5. The instruction that is used to complement or invert the bit of a bit addressable SFR is
   a) CLR C b) CPL C
   c) CPL Bit d) ANL Bit

Answer: c

6. The instructions that change the sequence of execution are
   a) conditional instructions
   b) logical instructions
   c) control transfer instructions
   d) data transfer instructions

Answer: c

7. The control transfer instructions are divided into
   a) explicit and implicit control transfer instructions
   b) conditional and unconditional control transfer instructions
   c) auto control and self control transfer instructions
   d) all of the mentioned

Answer: b

8. The conditional control transfer instructions check a bit condition which includes any bit of
   a) bit addressable RAM b) bit addressable SFRs
   c) content of accumulator d) all of the mentioned

Answer: d

9. All conditional jumps are
   a) absolute jumps b) long jumps
   c) short jumps d) none

Answer: c

10. The first byte of a short jump instruction represents
    a) opcode byte b) relative address
    c) opcode field d) none

Answer: a

11. In logical instructions, the immediate data can be an operand for
    a) increment operation b) decrement operation
    c) single operand instruction
    d) none

Answer: d

12. When we add two numbers the destination address must always be.
    a) some immediate data b) any register
    c) accumulator d) memory

Answer: c

13. DAA command adds 6 to the nibble if:
    a) CY and AC are necessarily 1
    b) either CY or AC is 1
    c) no relation with CY or AC
    d) CY is 1

Answer: b

14. If SUBB A,R4 is executed, then actually what operation is being applied?
    a) R4+A b) R4-A

c) A-R4 d) R4+A

Answer: c

15. A valid division instruction always makes:

a) CY=0, AC=1 b) CY=1, AC=1

c) CY=0, AC=0

d) no relation with AC and CY

Answer: c

16. In 8 bit signed number operations, OV flag is set to 1 if:

a) a carry is generated from D7 bit

b) a carry is generated from D3 bit

c) a carry is generated from D7 or D3 bit

d) a carry is generated from D7 or D6 bit

Answer: d

17. In unsigned number addition, the status of which bit is important?

a) OV b) CY

c) AC d) PSW

Answer: b

18. Which instructions have no effect on the flags of PSW?

a) ANL b) ORL

c) XRL d) All of the mentioned

Answer: d

19. ANL instruction is used _____

a) to AND the contents of the two registers

b) to mask the status of the bits

c) all of the mentioned

d) none of the mentioned

Answer: c

20. CJNE instruction makes _____

a) the pointer to jump if the values of the destination ar the source address are equal

b) sets CY=1, if the contents of the destination register are greater then that of the source register

c) sets CY=0, if the contents of the destination register are smaller then that of the source register

d) none of the mentioned

Answer: d

21. XRL, ORL, ANL commands have _____

a) accumulator as the destination address and any register, memory or any immediate data as the source address

b) accumulator as the destination address and any immediate data as the source address

c) any register as the destination address and accumulator, memory or any immediate data as the source address

d) any register as the destination address and any immediate data as the source address

Answer: a

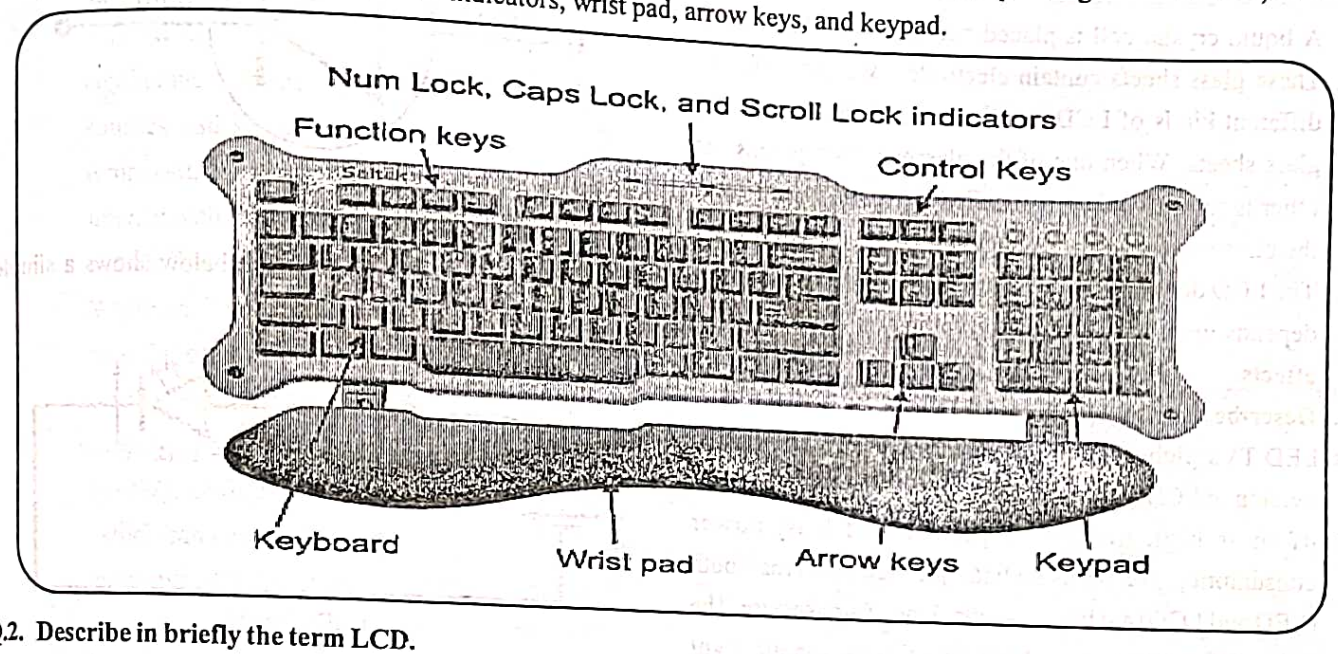
UNIT 03

MCS51 AND EXTERNAL INTERFACES & USER INTERFACE

Q1. Explain keyboard and its overview.

Ans. A keyboard is one of the primary input devices used with a computer. Similar to an electric typewriter, a keyboard is composed of buttons used to create letters, numbers, and symbols, and perform additional functions.

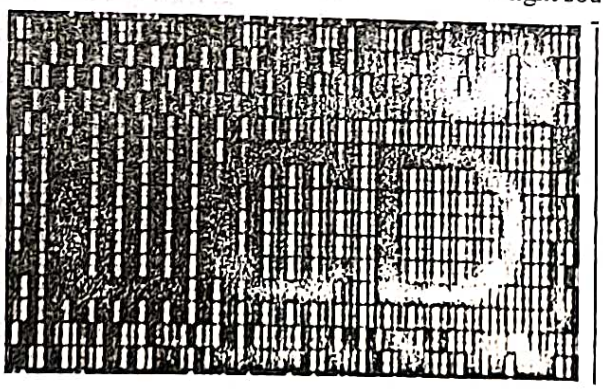
Keyboard overview : The following image shows a 104-key Saitek keyboard with arrows pointing to each section, including the control keys, function keys, LED indicators, wrist pad, arrow keys, and keypad.



Q.2. Describe in briefly the term LCD.

Ans. Liquid crystal is used as display device in LCD television. A series of cold cathode fluorescent (CCFL) is used at the back of the screen for providing light in LCD television.

CCFL is made up of long sealed glass tube having small diameter, inner phosphor coating and are filled with inert gas. A high voltage is applied across the tube. This causes the ionization of gases, which creates ultraviolet (UV) light that excites an inner coating of phosphor to produce visible light. CCFL is an excellent white light source, low cost and have long life.



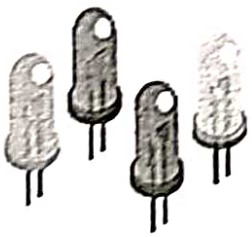
Liquid crystal display (LCD) is used now these days everywhere as display device. LCD is clearly replacing the CRT (cathode ray tube), because the size of CRT is bigger and it also draws large amount of power in comparison to LCD. LCD is made up of the liquid crystal.

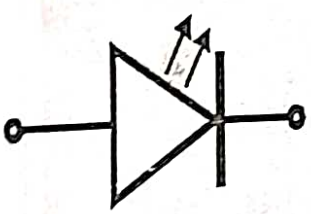
Liquid crystal is the combination of two states of matter-solid and liquid. It possess both the properties of solids and liquids and maintain their respective states with respect to another. The liquid crystal material shows more of a liquid state than that of a solid state. Liquid crystals are more heat sensitive than liquids. A little heat can transform liquid crystal into liquid.

A liquid crystal cell is placed between two glass sheets. These glass sheets contain electrodes. We can form two different kinds of LCDs on the basis of the selection of glass sheets. When one of the glasses is transparent and other is reflective then it is called reflective type. If both the glasses are transparent then it is called transitive type. The LCD does not produce luminance of itself. It entirely depends upon the illumination falling on it for its visual effects.

Q.3. Describe in briefly the term LED.

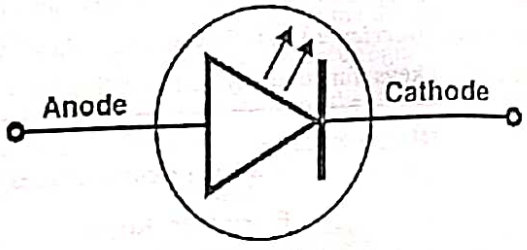
Ans. LED TVs (light-emitting diode televisions) are advanced version of LCD (liquid crystal display) televisions because of their high quality of picture and least power consumption. So far as technologies are concerned both (LED and LCD) are having similar kind of architecture. The only difference is that LED televisions contain light emitting diodes (LED) behind their screen. These LEDs provides sharper graphics and more illuminating effect upon the provision of current. CCFL (Cold cathode fluorescent lamp) used in LCD for the display which contains inert gas inside tube is producing desired light for the visual that is replaced by the LED in the LED television.





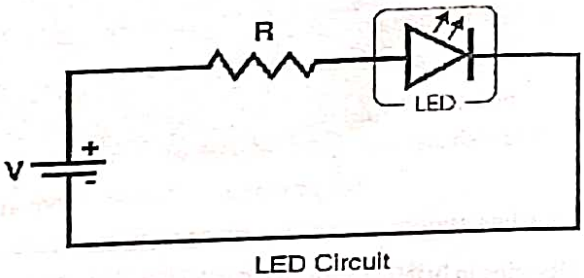
Light-emitting diodes are heavily doped p-n junctions. Based on the semiconductor material used and the amount of doping, an LED will emit a coloured light at a particular spectral wavelength when forward biased. As shown in the figure, an LED is encapsulated with a transparent cover so that emitted light can come out.

LED Symbol: The LED symbol is the standard symbol for a diode, with the addition of two small arrows denoting the emission of light.



LED Symbol

Simple LED Circuit: The figure below shows a simple LED circuit.



LED Circuit

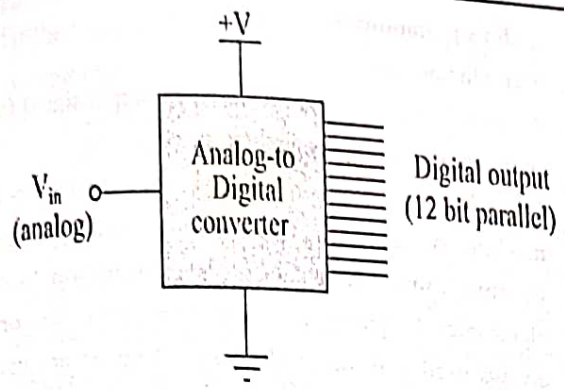
The circuit consists of an LED, a voltage supply and a resistor to regulate the current and voltage.

Advantages

1. Fine display of image.
2. Having better resolution and contrast.
3. Low power consumption.
4. Environmental friendly.
5. It is free from the defects of angle viewing which occurs in LCD.

Q4. Explain the term ADC.

Ans. Analogue to Digital Converter, or ADC, is a data converter which allows digital circuits to interface with the real world by encoding an analogue signal into a binary code

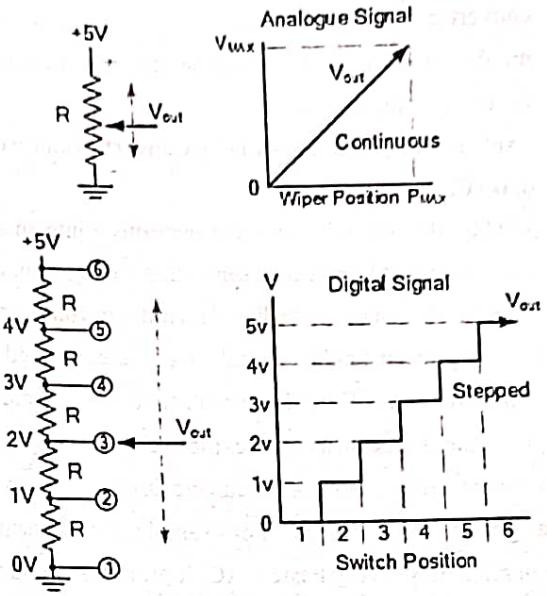


The Analogue-to-Digital Converter, (ADCs) allow micro-processor controlled circuits, Arduinos, Raspberry Pi, and other such digital logic circuits to communicate with the real world. In the real world, analogue signals have continuously changing values which come from various sources and sensors which can measure sound, light, temperature or movement, and many digital systems interact with their environment by measuring the analogue signals from such transducers.

While analogue signals can be continuous and provide an infinite number different voltage values, digital circuits on the other hand work with binary signal which have only two discrete states, a logic "1" (HIGH) or a logic "0" (LOW). So it is necessary to have an electronic circuit which can convert between the two different domains of continuously changing analogue signals and discrete digital signals, and this is where Analogue-to-Digital Converters (A/D) come in. Basically an analogue to digital converter takes a snapshot of an analogue voltage at one instant in time and produces a digital output code which represents this analogue voltage. The number of binary digits, or bits used to represent this analogue voltage value depends on the resolution of an A/D converter.

For example : A 4-bit ADC will have a resolution of one part in 15, (24 – 1) whereas an 8-bit ADC will have a resolution of one part in 255, (28 – 1). Thus an analogue to digital converter takes an unknown continuous analogue signal and converts it into an "n"- bit binary number of 2n bits. But first let us remind ourselves of the differences between an analogue (or analog) signal and a digital signal as shown:

Analogue and Digital Signals:



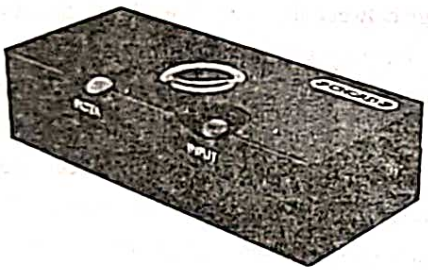
Here we can see that as the wiper terminal of the potentiometer is rotated between between 0 volts and VMAX, it produces a continuous output signal (or voltage) which has an infinite number of output values relative to the wiper position. As the potentiometers wiper is adjusted from one position to the next, there is no sudden or step change between the two voltage levels thereby producing a continuously variable output voltage.

Examples of analogue signals include temperature, pressure, liquid levels and light intensity. For a digital circuit the potentiometer wiper has been replaced by a single rotary switch which is connected in turn to each junction of the series resistor chain, forming a basic potential divider network. As the switch is rotated from one position (or node) to the next the output voltage, V_{OUT} changes quickly in discrete and distinctive voltage steps representing multiples of 1.0 volts on each switching action or step as shown. So for example, the output voltage will be 2 volts, 3 volts, 5 volts, etc. but NOT 2.5V, 3.1V or 4.6V. Finer output voltage levels could easily be produced by using a multi-positional switch and increasing the number of resistive elements within the potential divider network, therefore increasing the number of discrete switching steps. Then we can see that the major differences between an analogue signal and a digital signal is that an "Analogue" quantity is continuously changing over time while a "Digital" quantity has discrete (step by step) values.

"LOW" to "HIGH" or "HIGH" to "LOW". So how can we convert a continously changing signal with an infinite number of values to one which has distinct values or steps for use by a digital circuit.

Q5. Explain DAC(Digital-to-Analog Converter) and working of DAC.

Ans. A DAC takes digital data and transforms it into an analog audio signal. Afterward, it sends that analog signal to an amplifier. When you hear digital recordings, you're actually listening to an analog signal that was converted from digital by a DAC. Even if you can't see the DAC – although you sometimes can, as we'll explore shortly – it's there.As with most things audio-related, one DAC isn't necessarily as good as another DAC. For example, your smartphone contains only a very basic DAC. It produces sound that's "good enough" for you to carry on a conversation, but it's not optimal for getting the most from your favorite music recordings.Let's take a closer look at how DACs work and find out why investing in a high-quality one can help you achieve great sound.

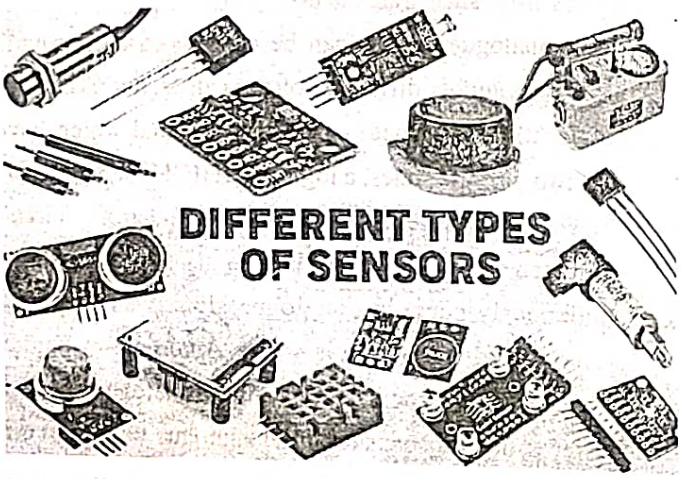


Fifty years ago, we didn't need DACs to produce an analog signal. Microphones inside a recording studio captured and stored sound as analog signals, usually in the form of reel to reel tape. The analog signal was then pressed into record grooves. Whenever you wanted to listen to a song, th needle on your turntable "felt" those grooves and created an electrical analog signal. It transmitted the signal through your preamp and, ultimately, your speakers.Today, recording engineers convert analog signals to a bitstream of numbers (ones and zeroes). That series of numbers is a digital audio signal. In order to listen to it, you need to convert it back to an analog signal.That's why we need DACs. Without them, we wouldn't be able to enjoy digital audio's portability and convenience.

Q6. Explain Sensors.

Ans. A sensor is a device that produces an output signal for the purpose of sensing a physical phenomenon.

In the broadest definition, a sensor is a device, module, machine, or subsystem that detects events or changes in its environment and sends the information to other electronics, frequently a computer processor. Sensors are always used with other electronics.Sensors are used in everyday objects such as touch-sensitive elevator buttons (tactile sensor) and lamps which dim or brighten by touching the base, and in innumerable applications of which most people are never aware. With advances in micromachinery and easy-to-use microcontroller platforms, the uses of sensors have expanded beyond the traditional fields of temperature, pressure and flow measurement, for example into MARG sensors.



Analog sensors such as potentiometers and force-sensing resistors are still widely used. Their applications include manufacturing and machinery, airplanes and aerospace, cars, medicine, robotics and many other aspects of our day-to-day life. There is a wide range of other sensors that measure chemical and physical properties of materials, including optical sensors for refractive index measurement, vibrational sensors for fluid viscosity measurement, and electro-chemical sensors for monitoring pH of fluids.A sensor's sensitivity indicates how much its output changes when the input quantity it measures changes. For instance,

if the mercury in a thermometer moves 1 cm when the temperature changes by 1 °C, its sensitivity is 1 cm/°C (it is basically the slope dy/dx assuming a linear characteristic). Some sensors can also affect what they measure; for instance, a room temperature thermometer inserted into a hot cup of liquid cools the liquid while the liquid heats the thermometer. Sensors are usually designed to have a small effect on what is measured; making the sensor smaller often improves this and may introduce other advantages.

Q7. Describe Communication interface.

Ans. Communications Interfaces means the interfaces and protocols that enable software installed on other computers (including servers and handheld devices) to interoperate with the Microsoft Platform Software on a Personal Computer.Communications Interfaces means the interfaces and protocols that enable software, directories, networks, Operating Systems, network Operating Systems or Web-Based Software installed on one computer (including Personal Computers, servers and Handheld Computing Devices) to Interoperate with the Microsoft Platform Software on another computer including without limitation communications designed to ensure security, authentication or privacy.

Examples of Communications Interfaces in a sentence : To achieve this security, Communications Interfaces to all meters must be located in a physically secure location and include strong password protection with either a network firewall or encrypted connection to limit the meter's network access to the PDP and/or a defined list of authorized users. As part of this disclosure, Microsoft shall identify, provide reasonable explanation of, and disseminate publicly a complete specification of all APIs, Communications Interfaces and Technical Information relating to the Interoperation of such Browser product(s) and/or functionality and each Microsoft Platform Software product. The purpose of this policy is to provide a standard for Health Net regarding communication interfaces ISS eNS1010POL - Network Security Use of Additional Communications Interfaces. Microsoft shall disclose to each OEM and Third-Party Licensee all APIs, Communications Interfaces and Technical Information necessary to permit them to fully exercise their rights under Section 2.c. Communications Interfaces Specify the various interfaces to communications such as local network protocols, etc. Communication system requirements are contained in a separate specification section as identified in paragraph entitled "Communications Interfaces". NI's hardware products include Data Acquisition Hardware, PXI Modular Instruments, Modular Instruments, Machine Vision/Image Acquisition, Motion Control, and NI LabVIEW Reconfigurable I/O (RIO) Architecture, Industrial Communications Interfaces, and GPIB Interface products. The new meter accurately measures power magnitude and direction, and can communicate as required by paragraph entitled "Communications Interfaces". The aforementioned license shall grant a royalty-free, non-exclusive perpetual right on a non-discriminatory basis to make, use, modify and distribute without limitation products implementing or derived from Microsoft's source code, and a royalty-free, non- exclusive perpetual right on a non-discriminatory basis to use any Microsoft APIs, Communications Interfaces and Technical Information used or called by Microsoft's Browser products or Browser functionality not otherwise covered by this paragraph. If the Court determines that Microsoft has undertaken such action, it shall issue an order enjoining Microsoft from asserting or enforcing any intellectual property rights in related APIs, Communications Interfaces, or Technical Information.

OBJECTIVE QUESTIONS ANSWERS

1. How many pins needed to generate I/O ports in 8051?

a) 30 b) 34

c) 32 d) 28

Answer: c

2. Find the contents of control word of the 8255 for the following configuration: All the ports of A, B and C are input ports (mode 1)

a) 3FH b) BFH

c) 9FH d) 1FH

Answer: b

3. In 8255, bit addressability is a available with port

a) A b) B

c) C d) D

Answer: c

4. Why interface chips are necessary in a microcontroller based system?

a) To solve the speed problem

b) To synchronize the data transfer between the CPU and I/O device

c) To synchronize the data transfer between the CPU and the I/O device, as well as to resolve the speed problem

d) None of the mentioned

Answer: c

5. Which of the following can be associated with bouncing contacts?

a) Push button switches b) Toggle Switches

c) Both push-button switches and toggle switches

d) Neither push-button switches not toggle switches

Answer: c

6. The term DIP in the phrase 'DIP switch' stands for

a) Double In-lane Package

b) Double In-line Package

c) Dual In-line Package

d) Dual In-lane Package

Answer: c

7. Find the control word of the 8255 for resetting BIT 4 of Port C

a) 00001111 b) 10001111

c) 10001000 d) 00001000

Answer: d

8. To get 2 displayed by a 7 segment display (common mode), what should be the combination of 8051 pins (P1.7 – P1.0)?

a) 01111101 b) 10111110

c) 01011011 d) 10100100

Answer: c

9. Which of the following is the correct combination to select port C in an 8255 chip?

a) CS = 0, A1 = 0, A0 = 0 b) CS = 0, A1 = 0, A0 = 1

c) CS = 0, A1 = 1, A0 = 0 d) CS = 1, A1 = 0, A0 = 0

Answer: c

10. What is the function of watchdog timer?

a) The watchdog Timers is an external timer that resets the system if the system if the software fails to operate properly.

b) The watchdog Timers is an internal timer that sets the system if the system if the software fails to operate properly.

c) The watchdog Timers is an internal timer that resets the system if the system if the software fails to operate properly.

d) None of the mentioned

Answer: c

11. In 8051, timer 1 run can be controlled by

a) TR1 b) TF1

c) IE1 d) IT1

Answer: a

12. The delay produced by 8051 mode 1 timer with TH = FF and TL = 00, crystal frequency 11.0592MHz is

a) 277.00 microsecond b) 277.76 microsecond

c) 278.00 microsecond d) 278.76 microsecond

Answer: b

13. 8051 counters in mode 2 are

a) 8 bit b) 16 bit

c) 12 bit d) Size Programmable

Answer: a

14. Which register in an 8051 microcontroller contains the SMOD bit?

a) SBUF b) TMOD

c) PCON d) TCON

Answer: c

15. In 8051, the instruction "MOV IP, #00000101" sets priorities of interrupts as

a) RI + TI > TF1 > INT0 > TF0 > INT1

b) TF1 > RI + TI > INT0 > TF0 > INT1

c) INT0 > INT1 > TF0 > TF1 > RI + TI

d) INT1 > INT0 > TF1 > TF0 > RI + TI

Answer: c

16. In Timer counter register of 8051, Mode 1 uses
a) 8-bit timer b) 16-bit timer
c) 13-bit timer d) 32-bit timer

Answer: b

17. What is the default interrupt priority in 8051?
a) INT0 > TF0 > RI+TI > INT1 > TF1
b) INT0 > TF1 > RI+TI > INT0 > TF0
c) INT0 > TF0 > INT1 > TF1 > RI + TI
d) INT1 > TF1 > INT0 > TF0 > RI + TI

Answer: c

18. Which bits in the PCON register of an 8051 microcontroller corresponds to the idle and power down modes?
a) PCON.0 – Idle mode, PCON.1 – Power down mode
b) PCON.1 – Idle mode, PCON.0 – Power down mode
c) PCON.0 – Idle mode/power down mode
d) PCON.1 – Idle mode/power down mode

Answer: a

19. In serial control (SCON) register, SCON.5 is used to
a) Transmit interrupt flag
b) Receive interrupt flag
c) Used for multi-processor communication
d) Receive enable

Answer: c

20. In idle mode of power control register, which of the following is not true?
a) All of registers, port and internal RAM maintain their data
b) The ALE and PSEN output are held low
c) The internal CPU clock is gated off
d) Interrupt, Timer and serial port functions act normally

Answer: b

21. 8 input DAC has
a) 8 Discrete voltage levels
b) 64 Discrete voltage levels
c) 128 Discrete voltage levels
d) 256 Discrete voltage levels

Answer: d

22. Which port is called a dedicated I/O port and which one is called a multi-functional I/O port in 8051?
a) Port 1 and port 3 b) Port 0 and port 2
c) Port 2 and port 3 d) Port 3 and port 1

Answer: a

23. How many SFRs related to timer/counter operation?
a) 3 b) 4
c) 5 d) 6

Answer: 6

24. Which one is a temperature sensor?
a) LM35 b) LM45
c) LM30 d) LM65

Answer: a

25. In 8051 microcontroller, Timer operating in mode 0, the timer register size is
a) 8 bit b) 13bit
c) 18bit d) 64bit

Answer: b

26. In 8051 microcontroller, show the bit that is used to start/stop the timer/counter?
a) Timer overflow b) Timer Run
c) Interrupt run d) Interrupt enable

Answer: b

27. In the TMOD register which bit is used to indicate timer 0/counter0 operation?
a) GATE b) C/T'
c) M1 d) M0

Answer: b

28. How many interrupts in 8051?
a) 4 b) 6
c) 5 d) 7

Answer: c

29. In the IP register, is it possible to give priority to all interruptions at a time?
a) Yes b) No

Answer: b

30. Which one of the following SFR is used for serial communication?

a) PCON b) TMOD
c) SMOD d) TCON

Answer: a

31. In the 8051 microcontrollers, What will be the timer clock frequency if the crystal frequency is 12 MHZ?
a) 1MHZ b) 12MHZ
c) 34MHZ d) 2MHZ

Answer: a

32. The timer1 operating in mode3 what will be the value loaded in the TMOD register?
a) 20H b) 30H
c) 34H d) 56H

Answer: b

33. To enable external interrupt 1which value to be loaded in the IE register?
a) 04H b) 05H
c) 06H d) 07H

Answer: a

34. In ADC interface with 8051 which hexa address is used to read ADC output?
a) C000H b) D000H
c) E000H d) F000H

Answer: c

35. For stepper motor interface which port of 8051 used for the forwarding operator?
a) Port 0 b) Port 1
c) Port 2 d) Port 3

Answer: c

36. SFRs location in internal RAM is
a) 70H TO 80H b) 80H to FFH
c) 00H to 80H d) 00H to 70H

Answer: b

37. EA' pin of 8051 is connected to VCC , the memory split up of program memory is,
a) 64Kb of internal ROM,0Kb of external memory
b) 0Kb of internal ROM,64Kb of external memory
c) 4Kb of internal ROM,60Kb of external memory
d) 4Kb of internal ROM,64Kb of external memory

Answer: c

38. 8051 Timers in Mode 1 configuration rolls over when it goes from _____.
a) FF to 00 b) 1FF to 000
c) 1FFF to 0000 d) FFFF to 0000

Answer: d

39. Which of the following interrupts in 8051 has the lowest priority?
a) External interrupt 0 b) Timer 1 interrupt
c) Serial port interrupts d) External interrupt 1

Answer: c

40. The asynchronous transmission always begins with _____.
a) Start bit b) Stop bit
c) Parity bit d) Sync bit

Answer: a

UNIT 04

C PROGRAMMING WITH 8051

Q.1. Explain I/O Programming in 8051.

Ans. In this section we look at C programming of the I/O ports for the 8051. We look at both byte and bit I/O programming.

Byte size I/O:

Ports PO – P3 are byte-accessible. We use the PO – P3 labels as defined in the 8051/52 C header file.

Bit-addressable I/O programming:The I/O ports of PO – P3 are bit-addressable. We can access a single bit without disturbing the rest of the port. We use the sbit data type to access a single bit of PO – P3'. One way to do that is to use the PxAy format where x is the port 0, 1, 2, or 3, and y is the bit 0 – 7 of that port. For example, P1A7 indicates PI.7. When using this method, you need to include the reg51 .h file.

Q2. Explain 8051 Timers and Counters.

Ans. The 8051 has two counters/timers which can be used either as timer to generate a time delay or as counter to count events happening outside the microcontroller.

The 8051 has two timers: timer 0 and timer1. They can be used either as timers or as counters. Both timers are 16 bits wide. Since the 8051 has an 8-bit architecture, each 16-bit is accessed as two separate registers of low byte and high byte. First we shall discuss about Timer 0 registers.

Timer 0 registers is a 16 bits register and accessed as low byte and high byte. The low byte is referred as a TL0 and the high byte is refer

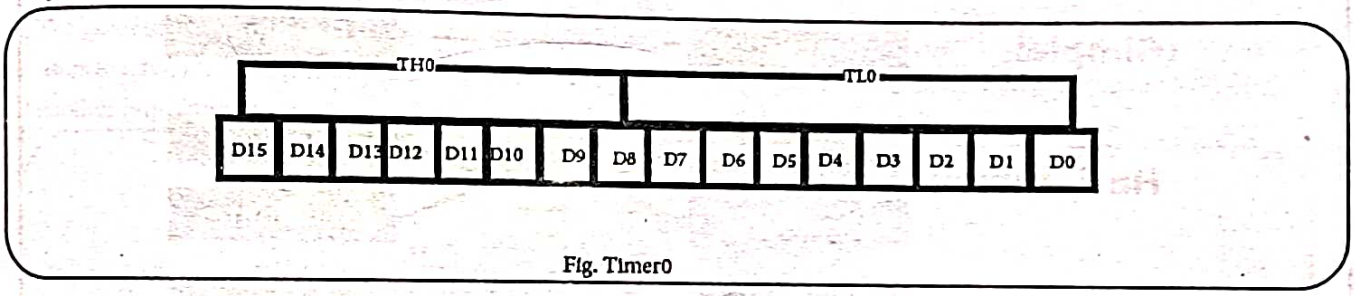


Fig. Timer0

Timer1 registers: is also a 16 bits register and is split into two bytes, referred to as TL1 and TH1.

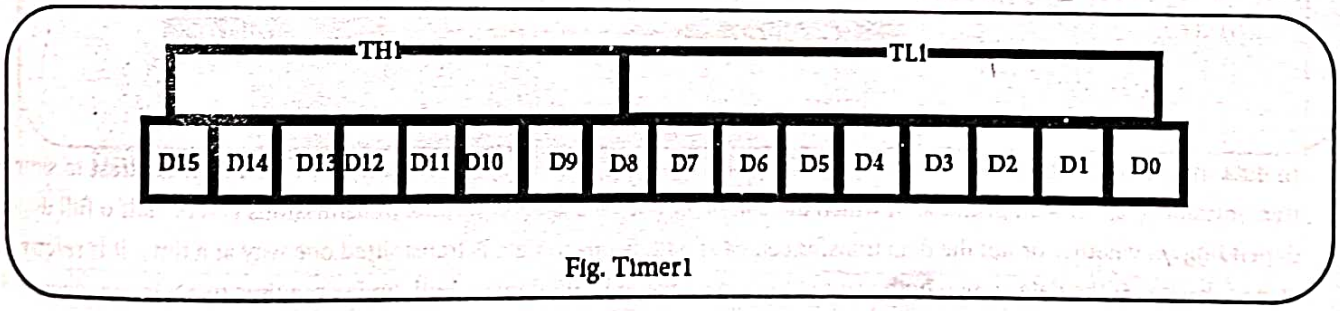


Fig. Timer1

Q3. Describe 8051 Serial Communication.

Ans. When a microcontroller communicates with the outside world, it provides the data in byte-sized chunks. In some cases, such as printers, the information is simply taken from the 8-bit data bus and presented to the 8-bit data bus of the printer. This can work only if the cable is not too long, since long cables diminish and even distort signals. Furthermore, an 8-bit data path is expensive. For these reasons, serial communication is used for transferring data between two systems located at distances of hundreds of feet to millions of miles apart. Fig(1) shows serial versus parallel data transfers. The fact that

serial communication uses a single data line instead of the 8-bit data line of parallel communication. For serial data communication to work, the byte of data must be converted to serial bits using a parallel-in-serial-out shift register, then it can be transmitted over a single data line. At the receiving end there must be a serial-in-parallel-out shift register to receive the serial data and pack them into a byte.

When the distance is short, the digital signal can be transferred as it is on a simple wire and requires no modulation. However, for long-distance data transfers, serial data communication requires a modem to modulate (convert to 0s and 1s to audio tones) and demodulate (converting from audio tones to 0s and 1s).

Serial data communication uses two methods, asynchronous and synchronous. The synchronous method transfers a block of data(characters) at a time, while the asynchronous method transfers a single byte at a time. There are special IC's made by many manufacturers for serial data communications. These chips are commonly referred to as UART (universal asynchronous receiver transmitter) and USART (universal synchronous asynchronous receiver transmitter).

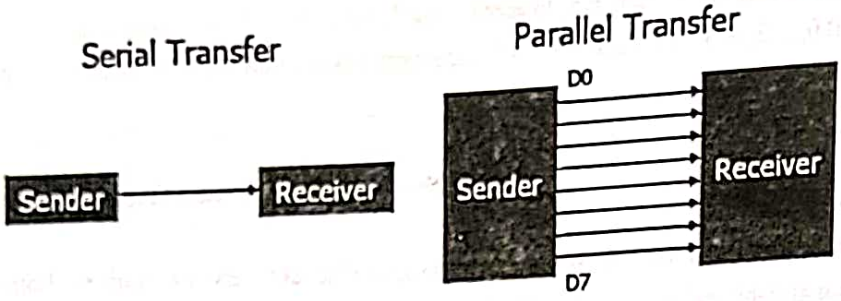


Fig.1

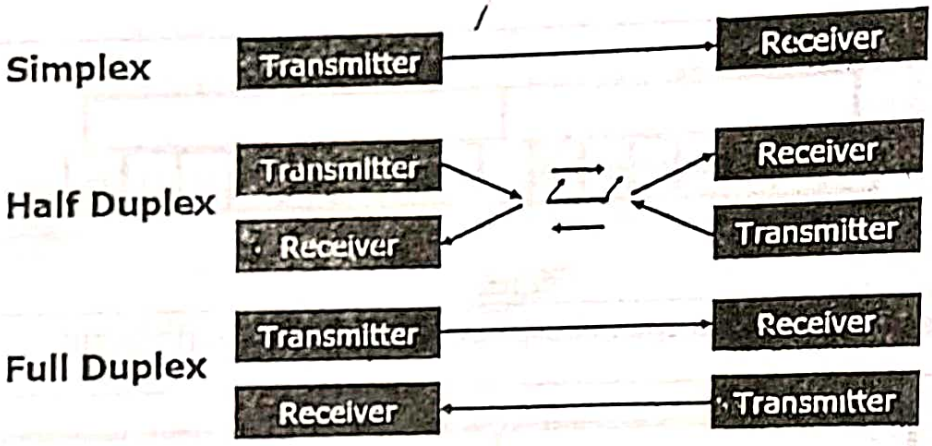


Fig. 2

In data transmission if the data can be transmitted and received, it is a duplex transmission. This is in contrast to simplex transmission such as with printers, in which the computer only sends data. Duplex transmissions can be half o full duplex, depending on whether or not the data transfer can be simultaneous. If data is transmitted one way at a time, it is referred to as half duplex. If the data can go both ways at the same time, it is full duplex. Full duplex requires two wire conductors for the data lines, one for transmission and one for reception, in order to transfer and receive data simultaneously.

Q4. Explain 8051 Interrupts.

Ans. Interrupts are the events that temporarily suspend the main program, pass the control to the external sources and execute their task. It then passes the control to the main program where it had left off.

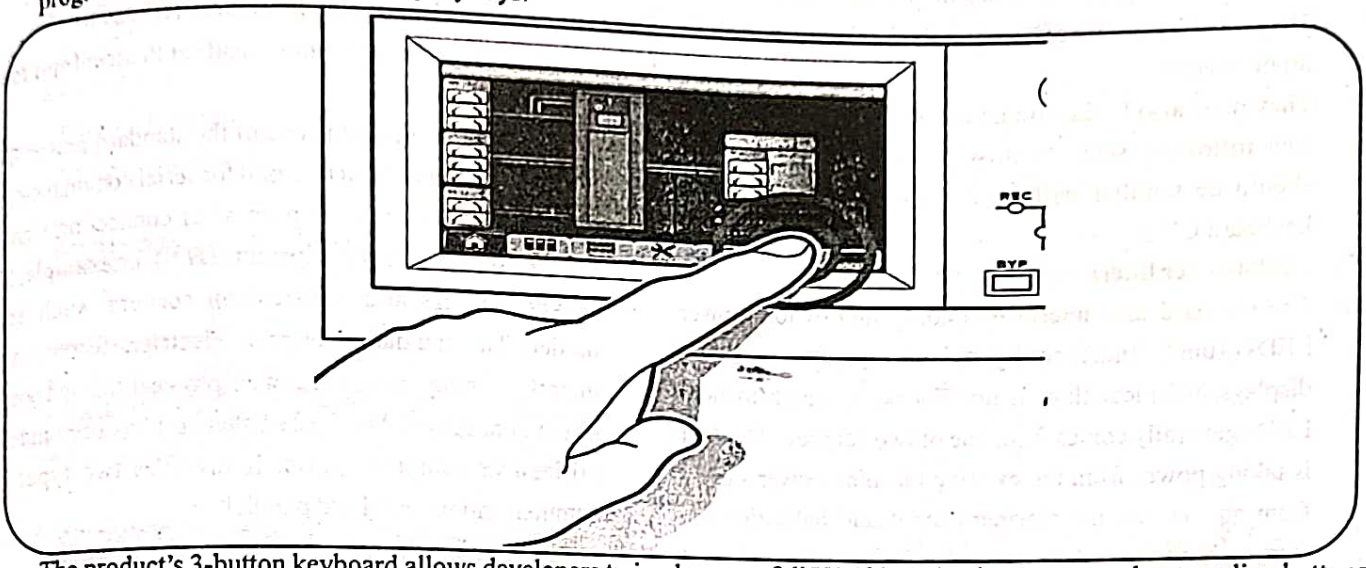
8051 has 5 interrupt signals, i.e. INT0, TF0, INT1, TF1, RI/TI. Each interrupt can be enabled or disabled by setting bits of the

IE register and the whole interrupt system can be disabled by clearing the EA bit of the same register.

Q5. **Describe LCD User Interface.**

Ans. LCD User Interface:

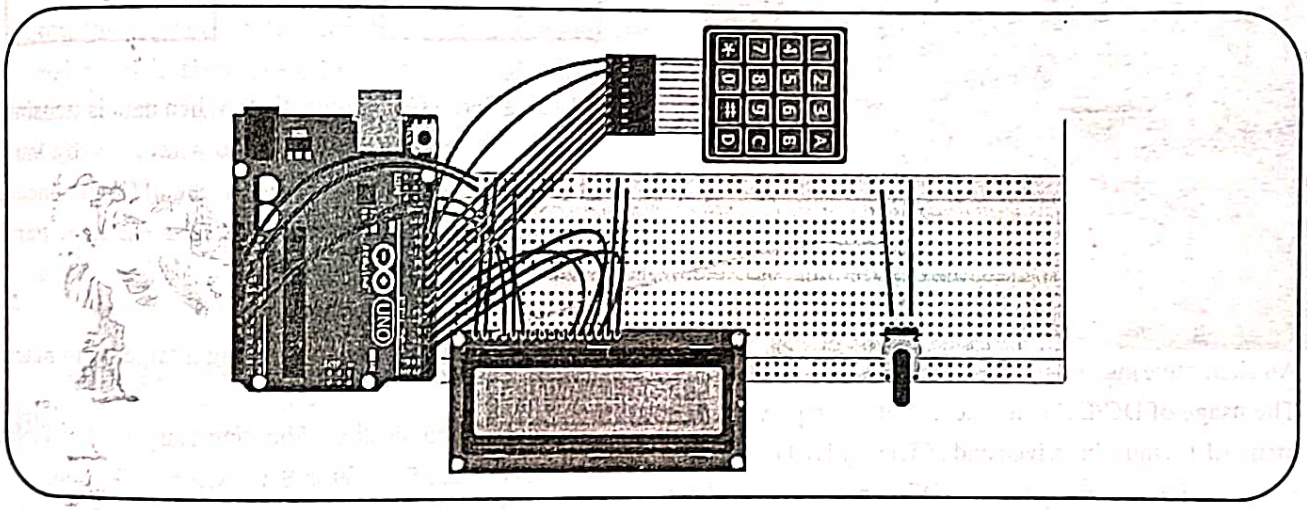
The programming-free LCD User Interface, which integrates onto any embedded platform and doesn't require LCD programming knowledge, the company says.



The product's 3-button keyboard allows developers to implement a full UI without having to worry about reading buttons, de-bouncing or programming resources on their host embedded system. The interface includes all control firmware on-board, utilizes a ARM M0 processor, and comes with free API. Included fonts and user-defined bitmaps allows for addition of 64K color displays. Display sizes begin at 1.77 inches, with larger sizes (2.8 and 5 inches) also available.

Q6. **Explain Keyboard User Interface Design.**

Ans. The guidelines for designing a keyboard user interface (UI) for a Microsoft Windows application. A keyboard UI allows users to navigate an application and manipulate UI elements by using a keyboard alone or in combination with a mouse (or another pointing device).



Following these guidelines will help you design a keyboard UI that makes your application more accessible to people with disabilities.

Role of the Keyboard UI in Accessibility:

A well-designed keyboard UI is an important aspect of software accessibility. It enables users who are blind or who have certain motor disabilities to navigate an application and interact with its features. Such users may be unable to operate a mouse, and may rely on assistive technologies such as keyboard enhancement tools, on-screen keyboards, screen enlargers,

screen readers, and voice input utilities all of which depend on an application's keyboard UI.

Fundamentals of Keyboard UI Design:

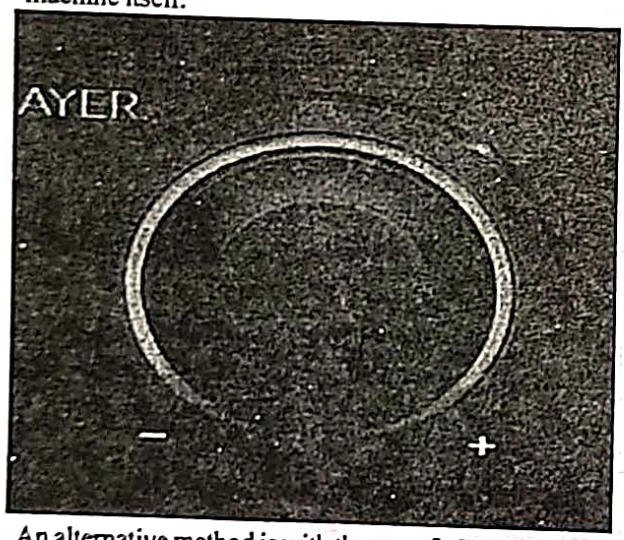
Well-designed applications include two basic requirements:

- They must be usable even when the keyboard is the sole input device.
- They must also be functional and user-friendly.

The following sections provide information that you should be familiar with before you begin to design a keyboard UI.

Q7. Explain User Interface.

Ans. The standard user interface is comprised of low power LEDs (10mA-20mA) configured in arrays, seven segment displays, or for icon illumination. The power supply to these LEDs generally comes from one of two sources. The first is taking power from the existing machine power supply from an existing transformer output and ballasting the current through a resistor network. This is often the lowest cost method as very few components are needed. One drawback however is that the energy loss can be significant and thus contributes to the loss of efficiency for the entire machine itself.

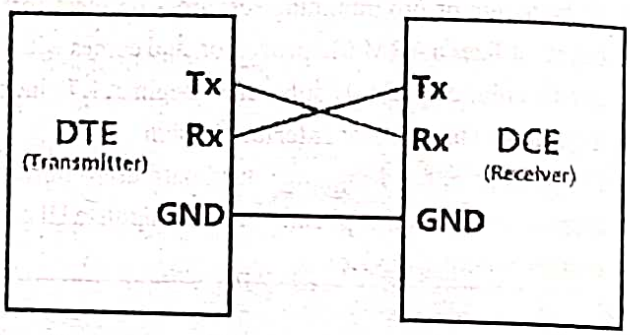


An alternative method is with the use of a DC/DC converter. The usage of DC/DC converters is often employed when many LEDs must be driven and efficiency is a key element of the design requirement. DC/DC converters also allow the standardization of power supplies so that one main power supply can be used for multiple product models, with the DC/DC adjusting its output based on the number of LEDs to be driven. Once the power supply configuration has been established, the next and most challenging step is to identify the best method of controlling the LEDs. Traditionally, three methods have been employed: direct drive from the MCU, control through serial communication, and advance serial control by dedicated LED drivers. Each method has its own benefits as well as drawbacks associated with it.

Q8. Describe communication interfaces (RS232).

Or, What is RS232 Serial Communication Protocol and How it Works?

Ans. What is RS232: RS232 is one of the standard protocol in telecommunication which is used for serial communication of data. It is basically the process of connecting signals between data terminal equipment (DTE) for example, file server, routers and application servers, such as a modem. The standard interprets electrical features and important timings of signal and the physical size and points of the connectors. The RS232 standard has been mostly utilized in computer ports. It involves two types of communication, serial and parallel.



What is Serial Communication: When data is transmitted bit by bit, from a transmitter to a receiver by various networking systems, it is known as Serial Communication. It is therefore a relatively slow process than Parallel Communication.

Example to understand:

Serial Communication – Shooting a target with machine gun.

Parallel Communication– Shooting a target with a shotgun.

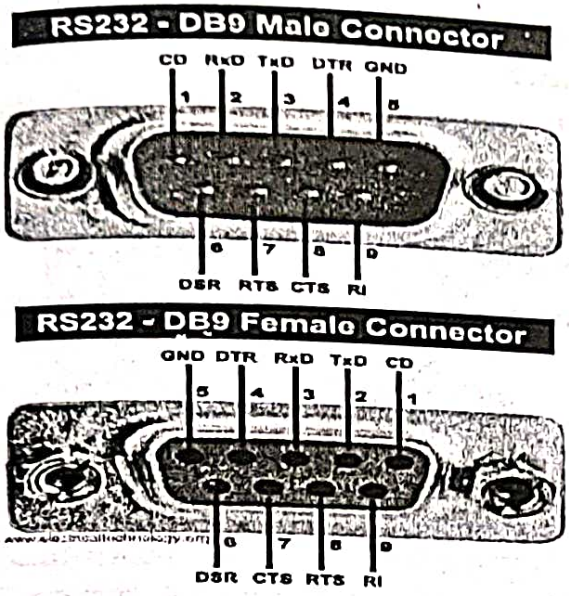
Modes of Data Transfer in Serial Communication:

Asynchronous Data Transfer – Bits of data are not synchronized by a clock pulse. Clock pulse is a signal utilized for synchronization of operation in an electronic systems.

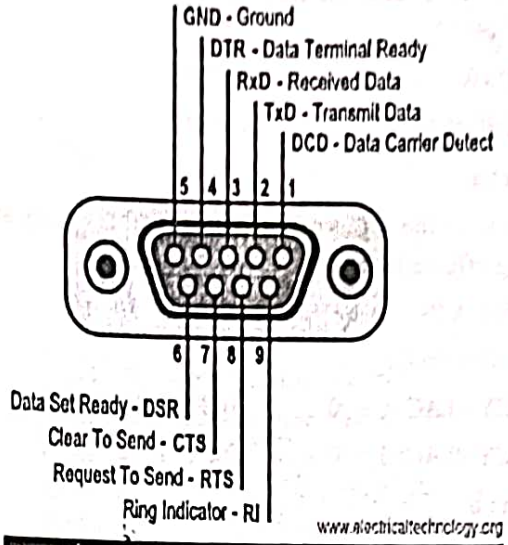
Synchronous Data Transfer – The mode in which the bits of data are synchronized by a clock pulse.

How RS232 Works: In RS232 standard devices one wire

transmits a changing voltage and other wire is connected to the ground as the wires has a single end. Noise induced by differences in ground voltages of driver and receiver circuit affects the Single-ended signals. The information or data in RS232 standard is serially transmitted only in one direction over a single data line. In order to incorporate a two way communication, three wires (RX, TX and GND) are needed along with the control signals. At any moment a byte of information can be passes given the fact, the previous byte of data has been transmitted already.



RS232 strictly follows asynchronous communication protocol i.e. there is no clock signal to synchronize the sender and receiver. Hence, it needs start and stop bits to inform the receiver when to check for data. There is a delay of certain time between the transmissions of each bit. This delay is an inactive state means the signal is set to -12 volts or logic "1" as mentioned earlier that logic 1 is -12 volts and logic 0 is 12 volts in RS232. First, the transmitter i.e. the DTE sends a Start bit to the receiver i.e. the DCE to inform it that data transmission starts from next bit. We always keep Start bit as logic 0 or +12 volts and the next 5 to 9 characters are the data bits.



RS232 - DB9 Female Connector Pinout

If parity bit is used, the maximum bits of 8 can be transmitted and if parity bit is not used then 9 data bits can be transmitted. After successfully sending the data the transmitter sends the stop bits which can be 1 bit, 2 bits or 5 bits long. Going by the fact that RS232 is a complete standard, many manufacturers does not follow the standards. Some of them abide by the complete identifications while some only partly follow the specifications. This is because this variation in implementation of the RS232 standard is that not all devices and applications require the full specifications and functionality of the RS232 Protocol. For instance, a serial model which is using a RS2323 may require more control lines than a serial mouse using the serial port.

OBJECTIVE QUESTIONS ANSWERS

1. 8051 microcontrollers are manufactured by which of the following companies?

a) Atmel b) Philips

c) Intel d) All of the mentioned

Answer: d

2. AT89C2051 has RAM of:

a) 128 bytes b) 256 bytes

c) 64 bytes d) 512 bytes

Answer: a

3. 8051 series has how many 16 bit registers?

a) 2 b) 3

c) 1 d) 0

Answer: a

4. When 8051 wakes up then 0x00 is loaded to which register?

a) PSW b) SP

c) PC d) None of the mentioned

Answer: c

5. When the microcontroller executes some arithmetic operations, then the flag bits of which register are affected?

a) PSW b) SP

c) DPTR d) PC

Answer: a

6. How are the status of the carry, auxiliary carry and parity flag affected if the write instruction

MOV A,#9C

ADD A,#64H

a) CY=0,AC=0,P=0 b) CY=1,AC=1,P=0

c) CY=0,AC=1,P=0 d) CY=1,AC=1,P=1

Answer: b

7. How are the bits of the register PSW affected if we select Bank2 of 8051?

a) PSW.5=0 and PSW.4=1

b) PSW.2=0 and PSW.3=1

c) PSW.3=1 and PSW.4=1

d) PSW.3=0 and PSW.4=1

Answer: d

8. If we push data onto the stack then the stack pointer

a) increases with every push

b) decreases with every push

c) increases & decreases with every push

d) none of the mentioned

Answer: a

9. On power up, the 8051 uses which RAM locations for register R0- R7

a) 00-2F b) 00-07

c) 00-7F d) 00-0F

Answer: b

10. How many bytes of bit addressable memory is present in 8051 based microcontrollers?

a) 8 bytes b) 32 bytes

c) 16 bytes d) 128 bytes

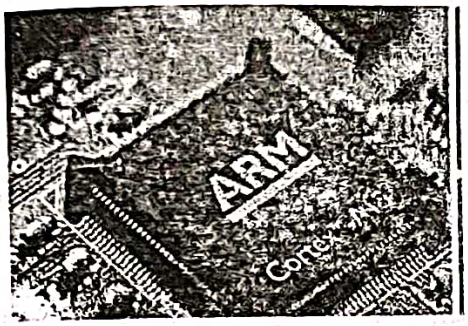
Answer: c

UNIT 05

ARM PROCESSOR

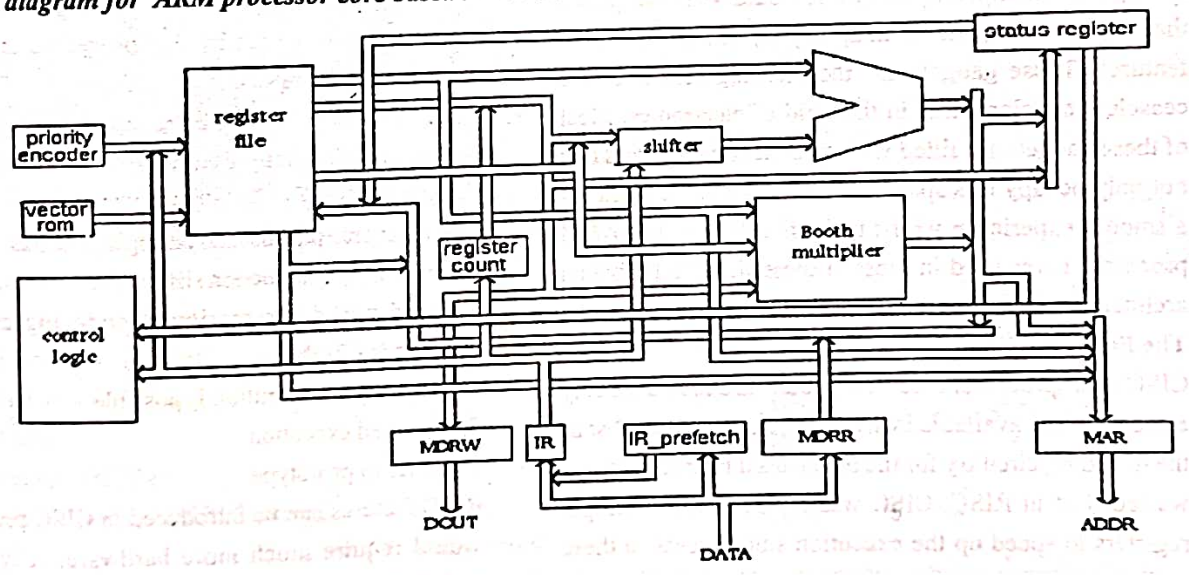
Q. 1. Describe the ARM processor core based microcontrollers and draw suitable block diagram for it.

Ans. Atmel ARM-based processors are microcontrollers and microprocessors integrated circuits, by Microchip Technology (previously Atmel), that are based on various 32-bit ARM processor cores, with in-house designed peripherals and tool support.



ARM licenses the core design for a series of 32-bit processors. ARM does not manufacture any complete silicon products, just intellectual property (IP). The ARM processors are RISC (reduced instruction set computing). This is similar to Microchip's AVR 8-bit products, a later adoption of RISC architecture. Whereas the AVR architecture used Harvard architecture exclusively, some ARM cores are Harvard (Cortex-M3) and others are Von Neumann architecture (ARM7TDMI). Semiconductor companies such as Microchip take the ARM cores, which use a consistent set of instructions and register naming, and add peripheral circuits such as ADCs (analog to digital converters), clock management, and serial communications such as USART, SPI, I2C, CAN, LIN, USB, Ethernet, and LCD, Camera or Touch controllers. Microchip made efforts to adapt advanced peripherals and power management that used very little power and can operate independently without having the CPU core powered up (sleepwalking). They also provided for DMA between external interfaces and memories increasing data throughput with minimal processor intervention. Microchip sells both MCUs microcontroller units) that have internal Flash memory, and MPUs (microprocessor units) that use external memory. In addition to the chips themselves, Microchip offers demo boards, both on its website, and through distribution channels such as Digi-key, Farnell, Ineltek, Arrow, Avnet, Future Electronics, and Mouser. ome of the Microchip ARM-based products are meant for specific applications, such as their SAM4CP that is used in smart-grid energy meters.

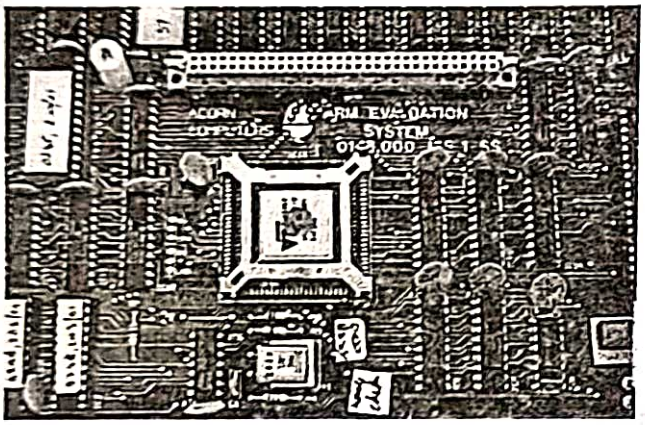
block diagram for ARM processor core based microcontrollers :



Q2. Explain the fundamentals of ARM processor and Berkeley RISC.

Ans. ARM is a family of instruction set architectures used in making computer processors developed by ARM Holdings. It is based on the reduced instruction set computing architecture which is commonly called as RISC. In 2010, ARM Holdings, plc reported shipments of approximately 6100 million ARM-based processors to manufacturers of chips based on ARM architectures, representing 35 per cent of digital TVs and set-top boxes, 95 per cent of smartphones and 10 per cent of mobile computers. As of 2014, ARM is the most widely used 32-bit instruction set architecture in terms of quantity produced.

Millions of electronic gadgets around the world invade our daily life and we have become completely dependent on them for performing most of our work.



A very nice example to justify this would be a smartphone that everyone is quickly adapting to, due to its varied features. These gadgets are the pleasing results of the ceaseless developments in the field of electronics. Most of these gadgets are fitted with embedded processors that not only occupy less space but also ensure that users get a smooth experience whilst using the device. The ARM processor cores used in most of these devices follow an architecture that helps them perform efficiently.

The Berkeley RISC:

CISC microprocessor cores like Motorola 68000 used only a subset of the available instruction set; therefore most of the decoding circuitry for the never-used instructions was wasted. But in RISC, CISC was replaced with multiple registers to speed up the execution since access to these registers would take less cycles than memory access needs, outperforming CISC.

Considering the case of ADD instructions in which CISC would appear in different formats where one would be meant for adding the numbers in two registers and placing the result in third, whilst the other would allow to add two numbers stored in the main memory and store the result in a register, offering wide variety of instructions to perform the required operations and providing several options for operands.

Processor Mode and Mode Number

Processor mode	Mode number	Description
User (usr)	0b10000	Normal program execution mode
FIQ (fiq)	0b10001	Supports a high-speed data transfer or channel process
IRQ (irq)	0b10010	Used for general-purpose interrupt handling
Supervisor (svc)	0b10011	A protected mode for the operating system
Abort (abt)	0b10111	Implements virtual memory and/or memory protection
Undefined (und)	0b11011	Supports emulation of hardware coprocessor
System (sys)	0b11111	Runs privileged operating system tasks (ARMv4 and above)

But in the case of RISC designs, the ADD would always take registers as operands, which creates a necessity for the programmer to write additional instructions to load the values from memory whenever required. Now, the Berkeley RISC was able to provide good performance utilising pipelining and register-windowing technique. In register windowing, the CPU contains a large number of registerss around 128, together called a register file, whilst the group of eight registers is called a window. But a program can only use one window, thereby allowing fast procedure calls. The call simply moves the window down to the set of eight registers used by that procedure and the return moves the window back.

After that time, RISC has seen a lot of developments proving its simplicity over CISC. Here are some of the features of RISC:

1. Large general-purpose 32-bit register banks
2. Fixed 32-bit instruction size
3. Hard-wired instruction decode logic instead of microcoded ROMs
4. Single-cycle execution is possible
5. Pipelined execution
6. Easier to prototype

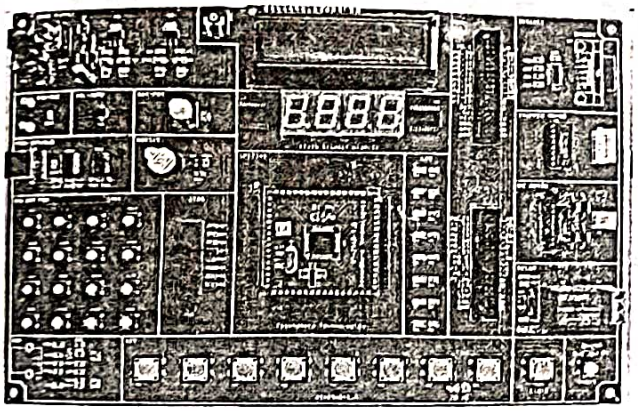
RISC features can be introduced in CISC processors but would require much more hardware. A typical RISC architecture consists of a large uniform register file, load

and store architecture, simple addressing modes and uniform fixed-length instruction fields. Due to this characteristic, we achieve high performance, low code size, low power consumption and low silicon area.

Q3. Explain ARM core based controller (LPC2148) and its features.

Or, ARM7 based LPC2148 Microcontroller and its features.

Ans. Embedded system and SOC (system on chip) designers choose particular microprocessor cores, libraries, and different tools to develop microprocessor based applications. An ARM processor is one of the best alternatives obtainable for embedded system designers. In the past few years, the ARM architecture has become very popular and these are available from different IC manufacturers. The applications of ARM processors involves in mobile phones, automotive braking systems, etc. A global ARM community partners have developed semiconductor as well as product-design corporations includes an employs like engineers, designers, & developers. This article is about ARM7 based LPC2148 microcontroller, architecture and pin configuration. This article will assist you to understand the basics of the microcontroller.



The LPC2148 microcontroller is designed by Philips (NXP Semiconductor) with several in-built features & peripherals. Due to these reasons, it will make more reliable as well as the efficient option for an application developer. LPC2148 is a 16-bit or 32-bit microcontroller based on ARM7 family.

Features of LPC2148:

The main features of LPC2148 include the following.

- The LPC2148 is a 16 bit or 32 bit ARM7 family based microcontroller and available in a small *LQFP64 package.
- ISP (in system programming) or IAP (in application programming) using on-chip boot loader software.
- On-chip static RAM is 8 kB-40 kB, on-chip flash memory is 32 kB-512 kB, the wide inter face is 128 bit, or accelerator allows 60 MHz high-speed operation.
- It takes 400 milliseconds time for erasing the data in full chip and 1 millisecond time for 256 bytes of programming.
- Embedded Trace interfaces and Embedded ICE RT offers real-time debugging with high-speed tracing of instruction execution and on-chip Real Monitor software.
- It has 2 kB of endpoint RAM and USB 2.0 full speed device controller. Furthermore, this microcontroller offers 8kB on-chip RAM nearby to USB with DMA.
- One or two 10-bit ADCs offer 6 or 14 analogs i/ps with low conversion time as 2.44 µs/ channel.
- Only 10 bit DAC offers changeable analog o/p.

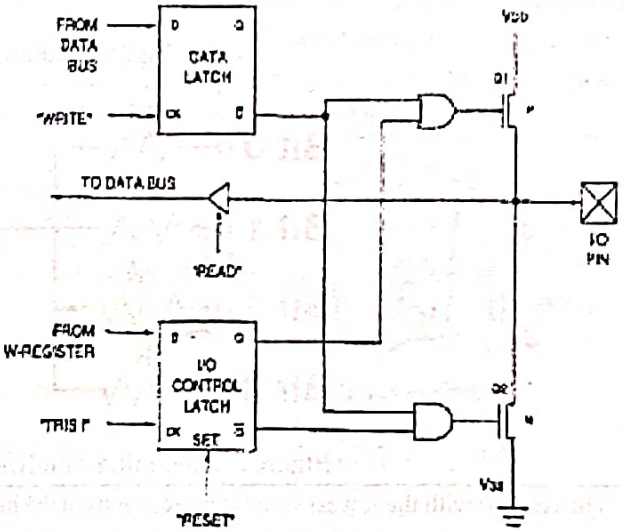
External event counter/32 bit timers-2, PWM unit, & watchdog. Low power RTC (real time clock) & 32 kHz clock input. Several serial interfaces like two 16C550 UARTs, two I2C-buses with 400 kbit/s speed. 5 volts tolerant quick general purpose Input/output pins in a small LQFP64 package. Outside interrupt pins-21.

Q4. Explain the term IO ports.

Ans. Input / Output Ports

To communicate with peripherals and other electronic devices, a computer needs to be able to input and output data beyond the computer itself. These pages explore the basics of computer I/O.

Bi-directional I/O



The diagram above shows a bit of a parallel bi-directional I/O port. This type of port provides both input and output

using the same port I/O pin (right). It may be used to provide a "bus" to connect peripherals. A control latch controls direction of the transfer (by setting a bit of the W (Write) register into the lower D type latch in the diagram. Below summary of the operations required to read data from a port pin:

Reading can be performed by using a move instruction to clock a '1' into the I/O control latch, which will (via the Q outp routed through the OR gate) switch OFF the upper FET (a p-channel type switches OFF when its input is high); simultaneou the '0' fed to the AND gate will switch OFF the lower FET. The output from the data latch is irrelevant as both FETs are of and the port is disabled . Data may now be read from the port pin. Write operations are a little more complex; we have consider the cases of writing a '0' and '1' separately. In either case we would use a move instruction to clock a '0' into the O control latch first, to configure the pin as an output.

Q5. Explain the term ADC and DAC

Ans. ***1.Digital to Analog Converter (DAC):*** In modern life, electronic equipment is frequently used in different fields such communication, transportation, entertainment, etc. Analog to Digital Converter (ADC) and Digital to Analog Converte (DAC) are very important components in electronic equipment. Since most real world signals are analog, these two convertin interfaces are necessary to allow digital electronic equipments to process the analog signals. Take the audio signal processin in Figure as an example, ADC converts the analog signal collected by audio input equipment, such as a microphone, int a digital signal that can be processed by computer. The computer may add sound effect such as echo and adjust the temp and pitch of the music. DAC converts the processed digital signal back into the analog signal that is used by audio outpu equipment such as a speaker.

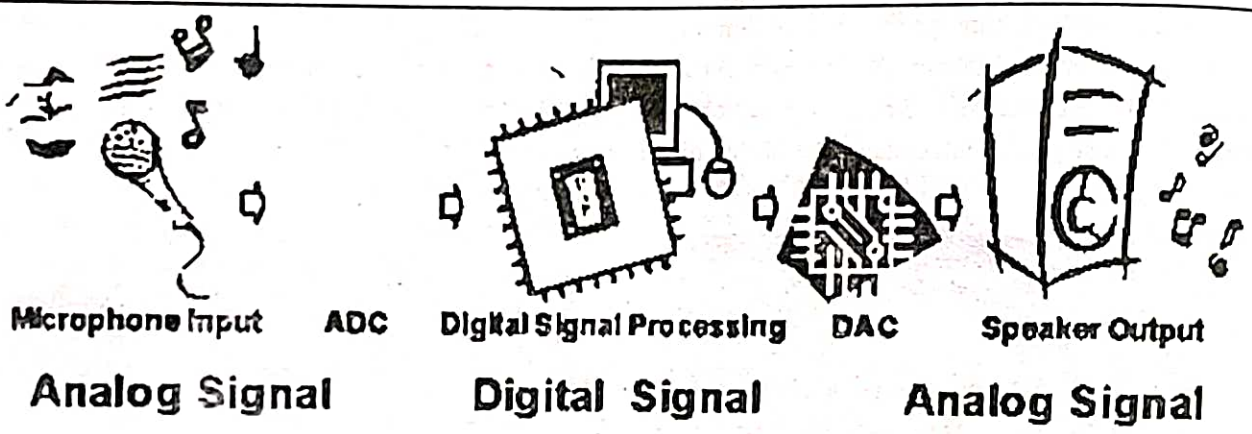


Figure : Audio signal processing

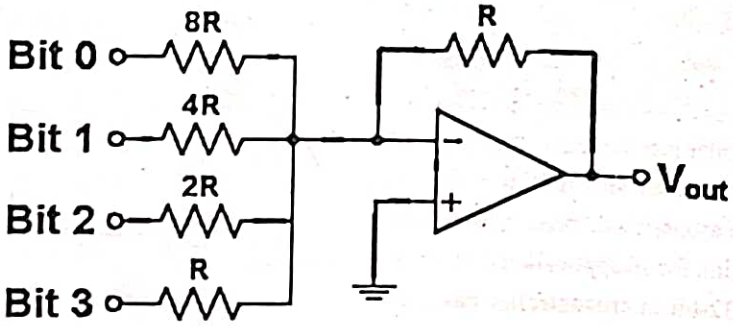


Figure : A Summing Amplifier functioning as a simple DAC

The resistor with the lowest value R corresponds to the highest weighted binary input Bit 3 (MSB) [23 = 8], and 2R, 4R, 8R correspond to the binary weights of Bit 2 (22 = 4), Bit 1 (21 = 2), and Bit 0 (LSB) [20 = 1] respectively. The relationship between the digital inputs (Bit 0 to Bit 3) and the analog output VOUT is as follow:

$$V_{OUT} = -V_{ref}\left(\frac{1}{1}Bit3 + \frac{1}{2}Bit2 + \frac{1}{4}Bit1 + \frac{1}{8}Bit0\right)$$

where Vref is the Reference Voltage of the circuit. Assuming the value of Vref as 5 V, the Analog Output Voltages corresponding to the Digital Input Codes is shown in Table 1.

Digital Input Code				Analog Output Voltage
Bit 3	Bit 2	Bit 1	Bit 0	(V)
0	0	0	0	0.000
0	0	0	1	-0.625
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375

Table 1: The Analog Output Voltages corresponding to the Digital Input Codes with Vref = 5 V

Analog To Digital Converter (ADC): In electronics, an Analog to Digital Converter (ADC) is a device for converting an analog signal (current, voltage etc.) to a digital code, usually binary. In the real world, most of the signals sensed and processed by humans are analog signals. Analog-to-Digital conversion is the primary means by which analog signal are converted into digital data that can be processed by computers for various purposes, Figure

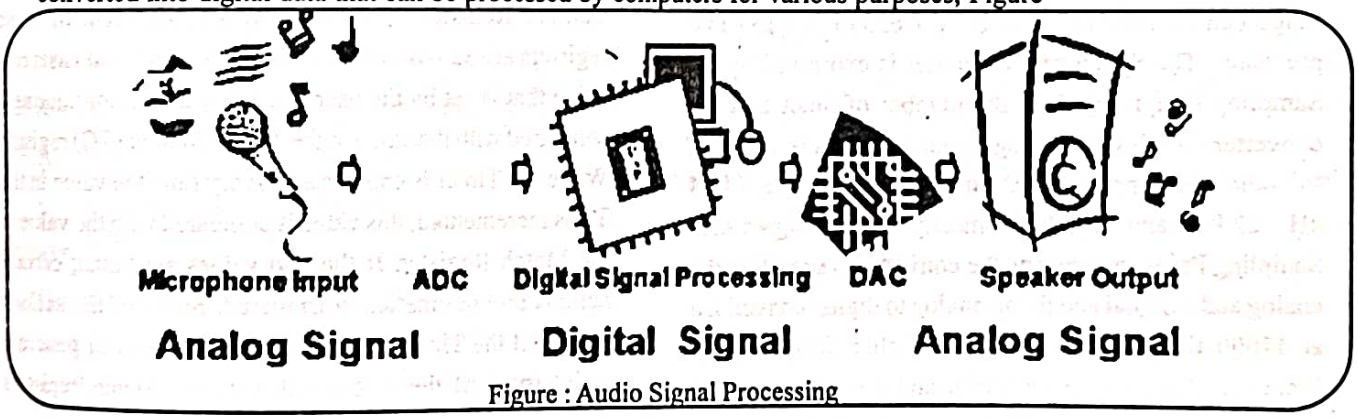


Figure : Audio Signal Processing

There are many types of ADC for different applications. The most inexpensive type of ADC is a Successive-Approximation ADC. Figure 4 shows the transfer curve of a 4-bit ADC. Inside a Successive-Approximation ADC, a series of digital codes, each corresponds to a fix analog level, are generated successively by an internal counter to compare with the analog signal

under conversion. The generation is stopped when the analog level becomes just larger than the analog signal. The digital code corresponds to the analog level is the desired digital representation of the analog signal.

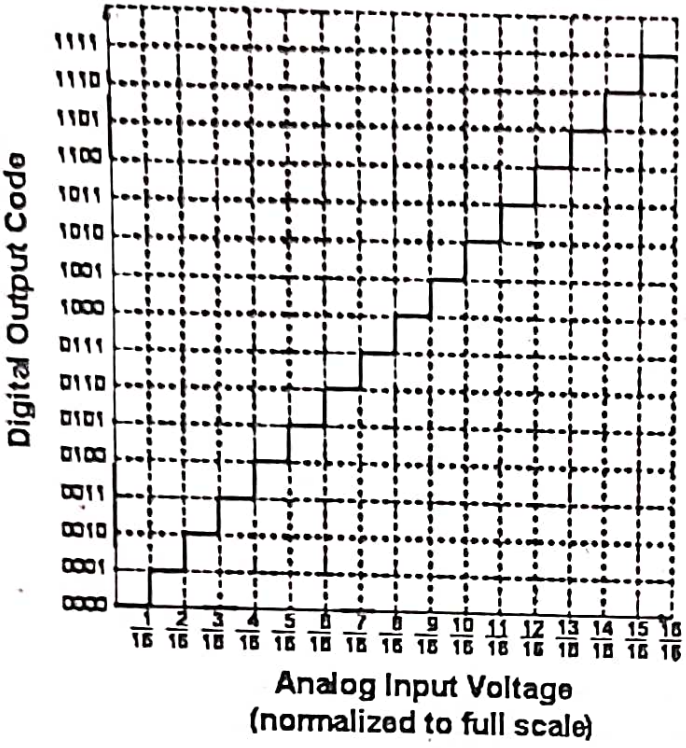


Figure : Ideal Transfer Curve of a 4-bit ADC

The performance of ADCs and DACs mainly depends on their Resolution and Speed. The Resolution of a converter is expressed in the number of Bit. For an ADC, the Resolution states the number of intervals or levels which can be divided from a certain analog input range. An n-bit ADC has the resolution of 1 / 2n. For example, the Resolution of a 16-bit ADC is 1 / 65536, since 216 = 65536. If the measuring voltage range is 10 V, then this input range can be resolved into 10 V / 65536 = 0.153 mV precision. The Speed of a converter is expressed by the Sampling Frequency. It is the number of times that the converter samples the analog signal, its unit is Hertz (Hz). In audio signal processing, Sampling Frequencies of 44 kHz, 22 kHz and 11 kHz are mostly used. Using 44 kHz Sampling Frequency means the converter is sampling the analog audio signal and doing analog to digital conversion at 44000 times per second. The higher the Sampling Frequency, the lower the distortion and the better the sound quality. ADCs are used virtually everywhere, whenever an analog signal has to be transported, it is processed and stored in digital form. They are always used together with different transducers to convert physical sense and measurement such as temperature, pressure, humidity, speed, vibration, sound, picture etc. in digital signal for further processing by microprocessor.

Q6. Explain the Timers / Counters in LPC2148.

Ans. Timers / Counters in LPC2148

There are two timer blocks in LPC2148 viz. Timer 0 / Counter 0 and Timer 1 / Counter 1. Both these timers are 32 – bit timers and both the blocks are identical except their base address is different. ither timer blocks can be used as a Timer for triggering an interrupt after certain time or as a Counter for counting the no. of external events or even demodulate the external PWM signals (through Capture inputs). Each timer block is associated with many registers but the two important registers are Timer Counter and Prescale Register. Both these registers work in coordination with each other. Prescale Register (PR) defines the resolution of the Timer. When a Timer block in the LPC2148 is reset and Enabled, the Timer Counter (TC) register is set to 0 and is incremented by 1 for every "PR + 1" clock cycles. When TC reaches the maximum value i.e. 0xFFFF FFFF, the value gets reset to 0x0000 0000 and starts counting again.

So, if PR is set to 0, the TC increments for every one clock cycle of the peripheral clock (PCLK). Similarly, if PR is set to 1, the TC increments for every two clock cycles of the peripheral clock. Hence, the value in the PR register determines when the timer increments or counts. Before going to discuss the other important registers associated with the Timers, we need to see about two important registers. Each Timer block has 4 Match Registers and 4 Capture Registers associated with them. Each of these registers are 32 – bit wide. The match register consists of a value that is set by the user and this value is continuously compared with the value in the Timer Counter (TC) register. When the Timer is enables and every time the value in the TC is incremented, this value is compared with the value in the Match Register. If the two values are equal, certain actions are automatically triggered. Some of the actions are Reset the Timer / Counter, stop the Timer or generate an interrupt. All the actions with respect to Match Registers are controlled using Match Control Register.

OBJECTIVE QUESTIONS ANSWERS

1). What is the standard form of ARM?

A. Advanced RISC Machine

B. Automatic RISC Machine

C. Automatic RISC Motor

D. None of the above

Answer: A

2). How many instruction sets does ARM have?

A. One B. Two

C. Three D. Four

Answer: D

3). How many registers does ARM have?

A. Four B. Eight

C. Sixteen D. Thirty-seven

Answer: D

4). How many operating modes does ARM have?

A. Four B. Seven

C. Sixteen D. Thirty-seven

Answer: B

5). When the processor is executing in ARM state, then all instructions are _____ wide

A. 8-bits B. 16-bits

C. 32-bits D. 64-bits

Answer: C

6). What is the standard form of LSL?

A. Logical Shift Left

B. Left Shift Logical

C. Logical Shift Logic

D. None of the above

Answer: A

7). How many arithmetic shift operators does ARM have?

A. One B. Two

C. Three D. Four

Answer: B

8). How many types of load instructions are there?

A. One B. Two

C. Three D. Four

Answer: C

9). How many classes of hazards are there?

A. One B. Two

C. Three D. Four

Answer: C

10). The OS timer is external peripheral in _____

A. ARM7/9 B. Cortex-M3

C. Both a and b D. None of the above

Answer: A

11). _____ are the hardware stacks in ARM7/9

A. FIQ, IRQ B. SVC, USR

C. ABT, UND D. All of the above

Answer: A

12). Which one of the following architecture has fewer number instructions?

A. RISC B. CISC

C. Both a and b D. None of the above

Answer: A

13). In which one of the following architecture the instructions are simple?

A. RISC B. CISC

C. Both a and b D. None of the above

Answer: A

14). The RISC processors execute _____ of instructions per second

A. Hundred B. Thousands

C. Millions D. None of the above

Answer: C

15). Which one of the following is a CISC architecture?

A. ARM7 B. 8051

C. Both a and b D. None of the above

Answer: B

16). When the processor is executing in thumb state, then all instructions are _____ wide

A. 8-bits B. 16-bits

C. 32-bits D. 64-bits

Answer: B

17). Which one of the following executes all instructions in one cycle?

A. ARM7 B. 8051
C. Both a and b D. None of the above

Answer: A

18). What is the standard form of LSR?

A. Logical Shift Right
B. Left Shift Right
C. Local Shift Right
D. None of the above

Answer: A

19). Which one of the following is the 8-bit controller?

A. ARM7 B. 8051
C. Both a and b D. None of the above

Answer: B

20). The ARM instruction set architecture divided into _____ classes of instructions

A. Two B. Four
C. Six D. Eight

Answer: C

21). What is the standard form of LPAE?

A. Large Page Address Extensions
B. Large Page Automatic Extensions
C. Large Page ARM Extensions
D. None of the above

Answer: A

22). _____ are the power saving techniques for ARM CPU's

A. RISC B. ISA optimization
C. Application-specific components
D. All of the above

Answer: D

23). When the processor is executing in jazelle state, then all instructions are _____ wide

A. 8-bits B. 16-bits
C. 32-bits D. 64-bits

Answer: A

24). What is the standard form of ASR?

A. Automatic Shift Right
B. ARM Shift Right
C. Arithmetic Shift Right
D. None of the above

Answer: C

25). What is the standard form of AMULET?

A. Asynchronous Microprocessor Using Low Energy Technology
B. Automatic Microprocessor Using Low Energy Technology
C. ARM Microprocessor Using Low Energy Technology
D. None of the above

Answer: A

26). The frequency of load/store instruction is around _____

A. 20% B. 10%
C. 40% D. 67%

Answer: D

27). In which year cortex R4 processor is introduced?

A. 2005 B. 2010
C. 2012 D. 2016

Answer: A

28). What is the standard form of ADK?

A. ARM Design Kit
B. Advanced Design Kit
C. AMBA Design Kit
D. None of the above

Answer: C

29). The branch with link, software interrupt, and general branch instructions are the _____ instructions

A. Branch B. Data processing
C. ARM D. None of the above

Answer: A

30). The typical clock rate of ARM9E is around _____

A. 100 MHZ (130nm)
B. 335 MHZ (130nm)
C. 266 MHZ (130nm)
D. None of the above

Answer: C